

Lowering software development costs by using Arm Cortex-M processors in an FPGA

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- Phillip Burr, Director of Embedded Portfolio, Arm
- Prakash Mohapatra, Senior Product Manager, Arm
- Lee Hansen, Senior Manager, Systems Software and SoC Technical Marketing, Xilinx

White Paper

Abstract— As design requirements and standards continue to evolve in the embedded market, FPGAs provide developers a great opportunity to get started on a project instantly, and incrementally improve the design over time. But how do you build a successful FPGA solution? Xilinx and Arm have joined forces to help embedded developers experience the benefits of a commercial FPGA, with the processing and software ecosystem of the Arm embedded processors. This paper illustrates how to use Cortex-M processors in Xilinx-based FPGAs and the key steps needed to take in order to develop a successful FPGA-based device, including integration, verification, synthesis and software development.

Introduction

Reprogrammable hardware is a key advantage for the electronics industry as it gravitates towards exploring means to optimize cost whilst retaining flexibility and without compromising on system performance. It is these advantages that are helping to drive the increased popularity of application-optimized designs. In many industries, such as automotive and industrial, the standards and protocols are dynamic and keep on evolving. Xilinx offers a wide array of reprogrammable hardware suited to a multitude of design needs from cost-optimized FPGAs, to radio frequency (RF) and embedded system-on-chip (SoC) designs, up to advanced ACAP (Adaptive Compute Accelerated Platforms). Gartner predicts 74% volume growth of the field programmable gate array (FPGA)/Programmable Logic Devices (PLD) market between 2016 and 2022 (Source: Gartner, Inc., Semiconductor Forecast Database, Worldwide, 2Q18 Update, July 2018).

In any embedded application project, software development adds significant cost and project time. Developers prefer to use existing software, where possible, and their choice of development tools and flow can have a huge impact on project timelines. Tools include debuggers and integrated development tools, for example, source decoders and linting options. Availability of an extensive ecosystem of proven software, knowledge articles, online documentation, and more can significantly improve the embedded software quality, and can reduce development time.

Arm offers the most extensive ecosystem of operating systems, tools, debuggers, compilers, Integrated Design Environments (IDEs), third-party libraries, middleware and developers for embedded systems. With over 130 billion Arm-based designs shipped to-date, the maturity and breadth of the ecosystem continues to increase, helping developers access wider choice and flexibility – key to reducing development costs and speeding time-to-market.

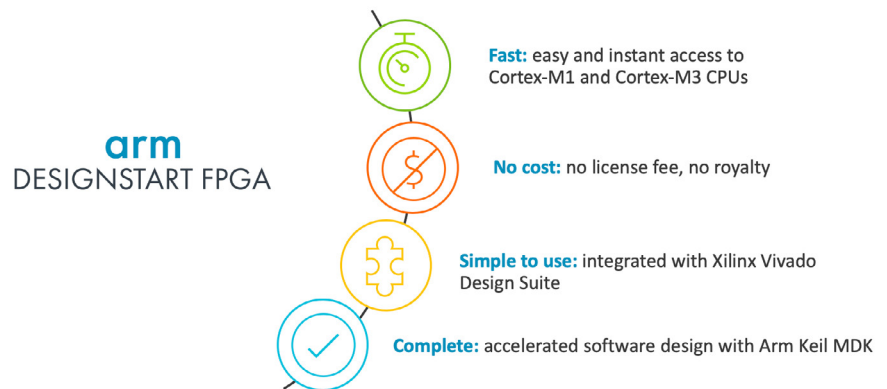
Arm Soft Processors on Xilinx FPGA

The availability of Arm's extensive software ecosystem on the most adopted FPGAs from Xilinx offers a tremendous boost to the embedded industry. The recent collaboration between Arm and Xilinx makes this possible. Now, developers have access to Arm soft-processor IP on Xilinx FPGA and SoC devices, and can take their projects to market quickly, without compromising on development risk and cost, through the Arm [DesignStart FPGA](#) program.

The essence of DesignStart is to offer developers an easy, instant and low-cost route to use Arm IP in their projects. For the last 10 years, DesignStart has helped companies accelerate innovation by reducing cost, time and entry barriers to application-optimized designs, such as custom SoC products. Now over 4,000 companies are evaluating this program worldwide at no cost, and more than 300 companies have accessed DesignStart for their commercial products for no upfront license fee.

The tremendous success and response from developers has encouraged Arm to open the benefits of Arm IP and its ecosystem to FPGA users. With DesignStart FPGA, Arm [Cortex-M1](#) and [Cortex-M3](#) soft CPU IP are available on Xilinx FPGAs, completely free of charge - there is no license fee and no royalty for using these CPUs on Xilinx devices. In addition, the CPUs are integrated with the Xilinx Vivado Design Suite for easy hardware design and board development.

Fig. 1:
Easy access to Arm
Cortex-M soft IP with
Xilinx FPGAs



All [Cortex-M processors](#) are 32-bit processors. Cortex-M1 is very similar to a Cortex-M0 processor; however, it is optimized for implementation on FPGA. Cortex-M1 implements the Armv6-M architecture, using a relatively small subset of the Arm Thumb instruction set. In Armv6-M, the instruction opcodes are almost all 16-bit in size, with a few double-opcode instructions of 32-bit. This optimized instruction set means that the code size is often smaller than even 8 or 16-bit processors resulting in smaller memory footprints, and hence, reducing system costs and power. This processor is ideal when you need a level of performance with minimal area. When the Cortex-M1 is implemented in the Xilinx Artix-7 FPGA (as used on the [Digilent Arty A7 development board](#)), it can reach a peak frequency of 100MHz.

The Cortex-M3 has been built to have a balance between performance and efficiency. Its Armv7-M instruction set is a superset of Armv6-M and includes more 32-bit opcodes to provide more computing capability per cycle. In SoC applications, its balance of power, performance, and area has made it widely applicable across a vast range of applications and consequently supported by a vast ecosystem of tools and users. The processor can reach a peak frequency of 50MHz when implemented on the Arty A7 board. This is a typical frequency for Cortex-M3 based MCU.

Designing Your FPGA

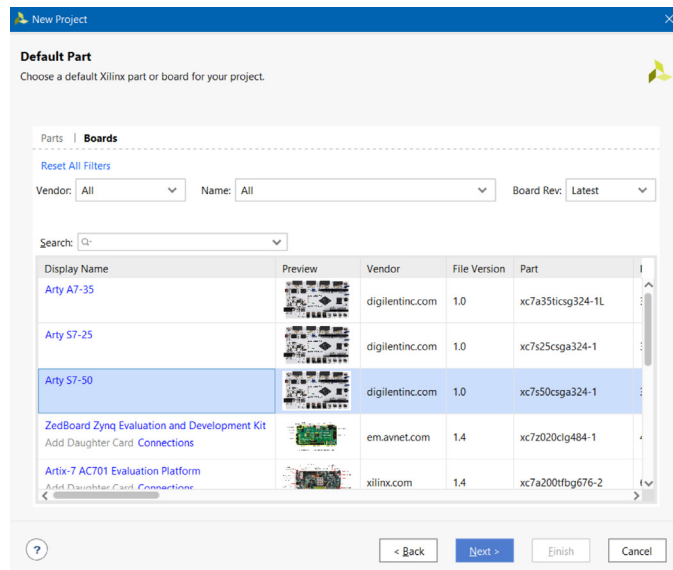
A. Integrating Cortex-M soft CPU IP in Xilinx FPGA

The Vivado HLx suites are the tools for completing hardware design on Xilinx target devices. It is available in three different editions, including the free Vivado HL WebPACK Edition supporting a variety of low-cost FPGA and SoC devices.

Vivado speeds the design process by letting designers apply board knowledge early, targeting either an existing development board platform or by letting designers define the

specific FPGA device and package for their project, delivering correct-by-construction designs from the very beginning of the flow. Alternatively, designers can start a basic design from scratch and apply device and/or board information later for maximum flexibility. DesignStart FPGA comes with example designs created for either the Digilent Arty A7 or Arty S7 development platforms, a cost-optimized set of boards that allows designers to try Cortex-M processors on the lowest-cost Xilinx FPGAs.

Fig. 2:
Choice of development
boards in Vivado



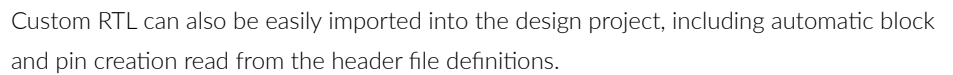
Vivado block designs allow developers to bypass the tedious step of manually connecting RTL, and in turn, speeding the design flow for common functions and connections. It allows developers to drag and drop IP from a vast configurable library of over 200 functions that include, but not limited to:

- + Simple adders and subtractors, UARTs and timers
- + Complex video IP such as interleave and image enhancement
- + Embedded functions such as mailbox and mutex communications
- + Peripherals such as tri-mode ethernet

With Cortex-M processors integrated with Vivado, these processors can be easily added to any design with a simple drag-and-drop. Once placed in the design, the Cortex-M component is configurable for many options, including, but not limited to:

- + Number of interrupts
- + Big or little endian
- + Debug type
- + Size of tightly-coupled instruction and data memory

Fig. 3:
Cortex-M1 configuration
option in Vivado

[illegible]

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interaction required; or can be highly user-driven through multiple command-line options and preferences, or timing constraints files and optional floor-planning. The flow is highly flexible to meet varied design expertise levels.

At the end of the hardware implementation, Vivado delivers a Hardware Definition File (HDF) containing all the relevant design information for software development tools, and a bitstream for programming the device. The design is then ready for application software development through a variety of tools such as the Xilinx Software Development Kit, [Arm Keil MDK](#), or IAR Workbench.

Software Ecosystem

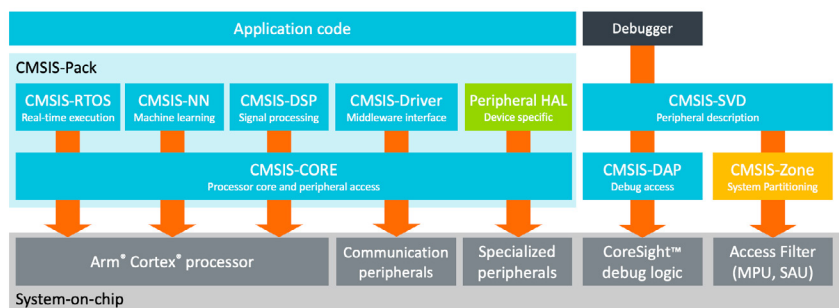
A. The Arm Software Ecosystem

With over 40 RTOS providers, 20+ IDE compilers and 21+ debug and trace solutions, the choice offered by Arm ecosystem is incredible. Arm-based development means it is easy to find the right tool or piece of software and at the right price point – from free to professional.

From a software perspective, Cortex-M processors have been built to remove the need for the user to write assembly code. This is enabled by the combination of the [Cortex-M Microcontroller Software Interface Standard \(CMSIS\)](#) and powerful compilers that optimize code written for Cortex-M processors in the high-level C language. In fact, there are around 8.5M downloads of CMSIS!

CMSIS provides a collection of API definitions, libraries, utilities, and methods that simplify and accelerate the creation of microcontroller applications. It is provided free-of-cost by Arm (and other contributors) with a permissive Apache 2.0 licenses and the software components can be used in any open source and commercial projects. It is an Open-source development on GitHub and the project can be [accessed here](#).

Fig. 5:
CMSIS architecture



| | |
|--------------|--|
| CMSIS-CORE | API for Cortex-M processor and core peripherals |
| CMSIS-DSP | DSP Math Library with more than 60 functions |
| CMSIS-SVD | XML system view description for peripheral debugging |
| CMSIS-RTOS | API for RTOS integration |
| CMSIS-DAP | Reference firmware for debug adaptors |
| CMSIS-DRIVER | API for peripheral driver interfaces |
| CMSIS-NN | Collection of efficient neural network kernels |
| CMSIS-ZONE | Methods to describe and partition system resources (multiple processors, memory area, peripherals, etc.) |
| CMSIS-PACK | XML description for software components, device parameters, board support |

Developers can benefit from RTOS, DSP-libraries, consistent access to peripheral, and debug visibility. Device vendors have a clear process to deploy support for new devices along with hardware abstraction layers and software libraries. CMSIS is supported by all leading toolchains and allows vendors to focus on the creation of the device. CMSIS offers a pathway to take advantage of the benefits of the extensive Arm ecosystem.

DesignStart FPGA provides access to the most comprehensive software development solution for Cortex-M: Arm Keil MDK. It contains the μ Vision IDE and debugger, the Arm compiler for superior code performance, and ready-to-use middleware. The debugger supports all advanced features for the soft processors: event recorder, component viewer, and event statistics. With DesignStart, you have access to free 90-day trial of MDK-Essential edition to help you accelerate software design.

Within the coming year, Xilinx will be introducing TCL-based script integration that will allow users to take the Hardware Definition File (HDF) output from Vivado and extract the necessary integration files for using Arm Keil MDK.

B. The Xilinx Software Ecosystem

Xilinx also provides a robust software development ecosystem and IDE based on the free eclipse-based Xilinx Software Development Kit (XSDK). This toolset directly imports the hardware definition HDF file from Vivado and extracts the software setup files that describe the system address map, and link together the driver files necessary for application development.

XSDK can create embedded applications targeted for any of Xilinx's platforms, currently on standalone bare-metal (no-OS). Open Source Linux (for use on Arm Cortex-A processors)

and FreeRTOS support will be added in incremental releases over the coming year. Third-party and custom OS vendors also offer a multitude of their own integration tools and IDE compatible with Vivado.

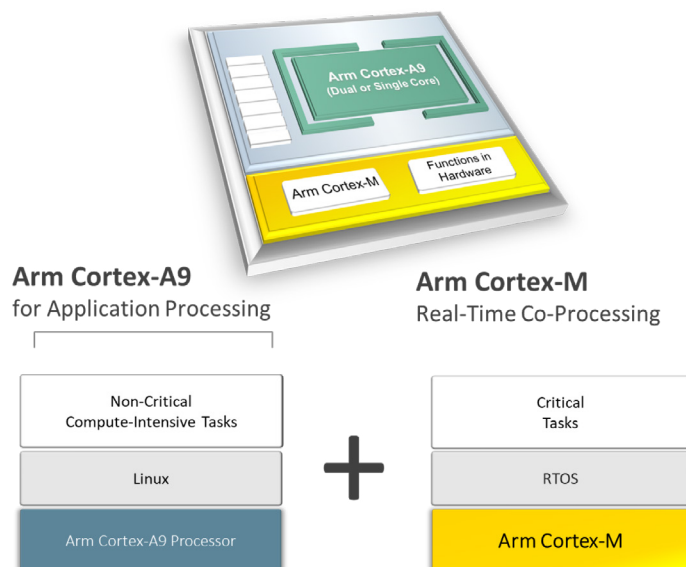
XSDK delivers IDE C/C++ source code creation and analysis, true heterogeneous multi-processor design, debug, and performance analysis options.

XSDK helps lower software development costs by providing features like direct-to-target board connections over JTAG, and connections through IP address for remote debug in a lab, in the field, or on the other side of the world. Users can modify application code in real-time, producing a new executable file in a matter of minutes, and try those changes on the board, for true real-time debug. There is also advanced feature support of hardware/software cross-triggering that allows for quick identification and correction of system-level issues.

Compute Offload

The Cortex-M processors can be used on any Xilinx device supported by Vivado, including the Zynq family of SoCs, enabling the Cortex-M to be used as an offload engine.

Fig. 6:
Zynq family with Cortex-M
soft processors



The Arm Cortex-A9 hard processor in the Zynq FPGA can run compute-intensive and application tasks; whereas the Cortex-M can be utilized for real-time tasks such as industrial automation, motor control, etc. While the Cortex-A9 can have a rich operating system such as Linux; the Cortex-M can run a RTOS for bounded interrupt latency.

Conclusion

Adding single or multiple Arm Cortex-M microcontrollers to Xilinx FPGA or SoCs is now much simpler and open to all embedded developers. The Arm and Xilinx partnership delivers proven Cortex-M soft processors, an extensive software ecosystem, and the Vivado Design Suite, coupled with low-cost Xilinx FPGAs and SoCs. This combination makes flexible embedded hardware and application development fast and easy, without compromising on cost constraints.

For further reading or additional resources, please use the links below:

- + [Tutorials, videos and documentation for integrating Cortex-M soft IP on Xilinx FPGA](#)
- + [Arm Keil MDK for DesignStart](#)
- + [Resources for CMSIS](#)
- + [Xilinx Vivado Design Suite](#)
- + [Xilinx Software Development Kit](#)



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