

Certificate



Functional
Safety

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ID 060000000

No.: 968/FSP 2448.01/24

Product tested General purpose microprocessor IP including safety features **Certificate holder** ARM Ltd.
110 Fulbourn Road
Cherry Hinton
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Type designation ARM Cortex-R52+ Processor IP Core
Approved versions, see current Revision List

Codes and standards IEC 61508 Parts 1-7:2010 (in extracts) ISO 26262-8:2018
ISO 26262-2:2018 ISO 26262-9:2018
ISO 26262-5:2018

Intended application The ARM Cortex-R52+ Processor IP Core complies with the requirements of IEC 61508 for SIL 3 regarding the avoidance of systematic faults for a Compliant Item and complies with the requirements of ISO 26262 for ASIL D regarding the avoidance of systematic faults for a Safety-Element-out-of-Context (SEooC).

Based on an exemplary configuration, ARM showed that the target values for the random hardware fault metrics according to ISO 26262-5, Clauses 8 and 9 for ASIL D can be met. As a result, the Cortex-R52+ Processor can be used in safety-related applications up to SIL 3 according IEC 61508 and up to ASIL D according to ISO 26262.

Specific requirements The requirements and constraints specified in the Cortex-R52+ Safety Manual have to be taken into account by the user.

The issue of this certificate is based upon an evaluation in accordance with the Certification Programs CERT FSP1 V3.0:2020, CERT FSP2 V3.0:2020 in their actual version, whose results are documented in Report No. 968/FSP 2448.01/24 dated 2024-04-19. This certificate is valid only for products, which are identical with the product tested. Issued by the certification body accredited by DAkkS according to DIN EN ISO/IEC 17065. The accreditation is only valid for the scope listed in the annex to the accreditation certificate D-ZE-11052-02-00.

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Köln, 2024-04-22

Certification Body Safety & Security for Automation & Grid

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