Certificate / Certificat

Zertifikat / 合格証

Arm 2103-105 C022

exida hereby confirms that the:

Arm Cortex-M55 Processor

Arm Ltd.
Cambridge, Great Britain

Has been assessed per the relevant requirements of:

ISO 26262:2018 Parts 2, 4, 5, 7, 8 and 9

IEC 61508:2010 Parts 1 and 2

and meets the requirements providing a level of integrity to:

Systematic Capability: ASIL D / SIL 3 Capable

Safety related function:

The Cortex-M55 Processor was developed as a HW Safety Element out of Context (SEooC) or compliant item, with the assumption that the following functions will be used in a safety related application context:

- Execution of instructions, generating the correct result and executing in the right order
- Correct response to stimuli like interrupts and events
- Correct usage of buses according to defined protocols
- Correct usage of coprocessors with a defined interface

Application restrictions:

The Cortex-M55 processor shall be used according to the requirements described in the Arm Cortex-M55 Processor Safety Manual.

The manufacturer may use the mark:

Revision 2.0 Nov 28, 2024
Surveillance Audit Due
Mar 1, 2026

ANSI National Accreditation Board
ACCREDITED
ISO/IEC 17065
PRODUCT CERTIFICATION BODY
#1004

exida Certification

Evaluating Assessor

Certifying Assessor

Arm Cortex-M55 Processor

Certificate / Certificat / Zertifikat / 合格証

Arm Cortex-M55 Processor

Systematic Capability: ASIL D / SIL 3 Capable

Product Overview

The Arm® Cortex®-M55 Processor is a synthesizable soft-IP (i.e. RTL code) for integration into a safety related IC or SoC (system-on-chip). To support safety related applications, the Cortex-M55 includes several safety mechanisms to detect and control hardware faults (e.g. Dual-Core Lockstep, SECDED ECC for memories and caches, Flop parity, etc.), or to prevent and control systematic failures on SoC and software level (e.g. Memory Protection Unit, etc.).

Systematic Capability: ASIL D / SC 3 (SIL 3 Capable)

The Arm Cortex-M55 Processor has been developed as a Hardware Safety Element out of Context (SEooC) or compliant item according to ISO 26262-10 and IEC 610508-2. The development, as documented by Arm, meets the applicable ASIL D requirements for specification, implementation and verification from ISO 26262 parts 4, 5 and 7–9, as guided by ISO 26262-10 and the functional safety management requirements of ISO 26262-2. It also meets the applicable requirements for SIL 3 capability (SC 3) from IEC 61508 parts 1 and 2.

Hardware Safety Integrity: ASIL D / SIL 3 (HFT=0) or ASIL B / SIL 2 (HFT=0)

The Arm Cortex-M55 Processor can be configured to include different safety mechanisms, to target different use cases and safety integrity levels. According to IEC 61508-2, it is a Type B element without hardware fault tolerance (HFT=0).

The FMEDA results show that the Cortex-M55 Processor, when used in a DCLS (dual-core lockstep) configuration, fulfills the ASIL D requirements of ISO 26262-5, clause 8, including the ASIL D target values for the architectural metrics SPFM and LFM, and it can also fulfill the SIL 3 requirements of IEC 61508-2, table 3, including the SIL 3 target value for the SFF architectural metric.

The FMEDA results show further that the Cortex-M55 Processor, when used in a single-core configuration together with STL (Software Test Library), achieves the following architectural metric results for the CPU logic (excluding memories):

Functional Safety Standard	Permanent Faults	Transient Faults
ISO 26262-5, Clause 8	SPFM = 78%	SPFM = 98%
IEC 61508-2, Clause 7.4.4	SFF = 76%	SFF = 92%

This means that when integrated together with ECC protected internal memories, per the requirements given in the Safety Manuals, ASIL B / SIL 2 metric target values may be achieved overall, depending on the configuration.

It is the responsibility of the Cortex-M55 integrator to adjust the FMEDA to their actual IP configuration, to determine STL diagnostic coverage for their exact IP configuration by re-running fault injection simulation on gate-level netlist, and to re-evaluate the FMEDA results in the context of their safety related IC or SoC.

The following documents are a mandatory part of this certification:

Assessment Report: Arm 21/03-105 R021, V2 R0
Safety Manual: Arm Cortex-M55 Processor Safety Manual,
Arm Cortex-M55 Processor STL Safety Manual
FMEDA Report: Arm Cortex-M55 Processor FMEDA Report
Arm Cortex-M55 Processor STL FMEDA Report

80 N Main St
Sellersville, PA 18960