SYNOPSYS®
Silicon to Software™

Best Practices using Synopsys Fusion Technology to Achieve High-performance, Energy Efficient implementations of the latest Arm® Processors in TSMC 7-nanometer FinFET (7FF) Process Technology

Leah Schuth - Arm
Mike Montana - Synopsys

October 2019

Agenda

Challenges on the Horizon

Synopsys Fusion Compiler

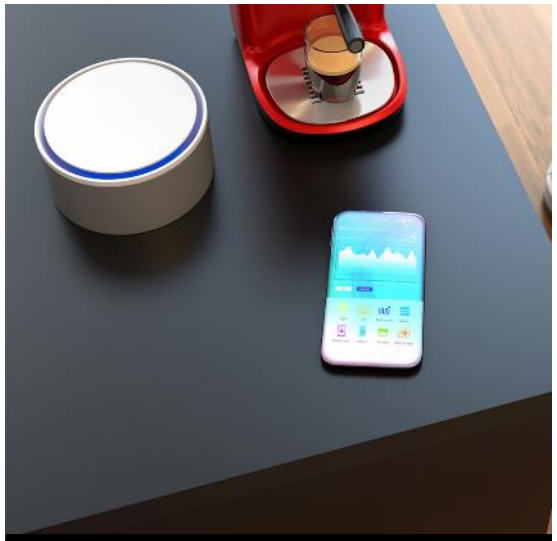
Deploying Fusion Compiler for Arm CPU

An Arm Perspective on Technology Trends and Solutions

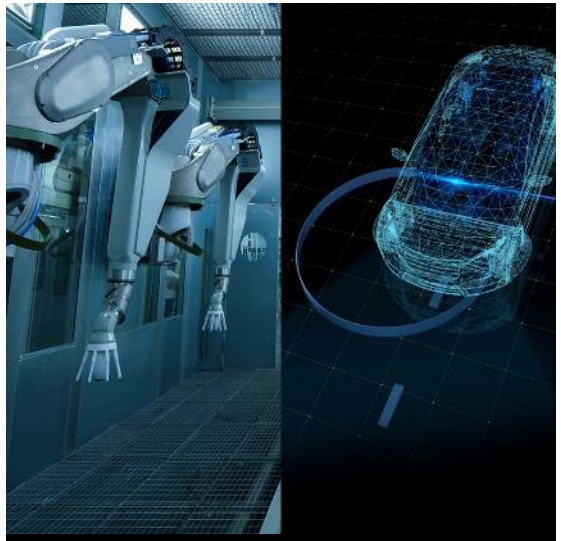
Leah Schuth

Director, Technical Marketing, Physical Design Group

Technology trends that will redefine all industries



Artificial Intelligence in every device



Autonomous machines

Augmented reality

Hyperscale cloud and connectivity

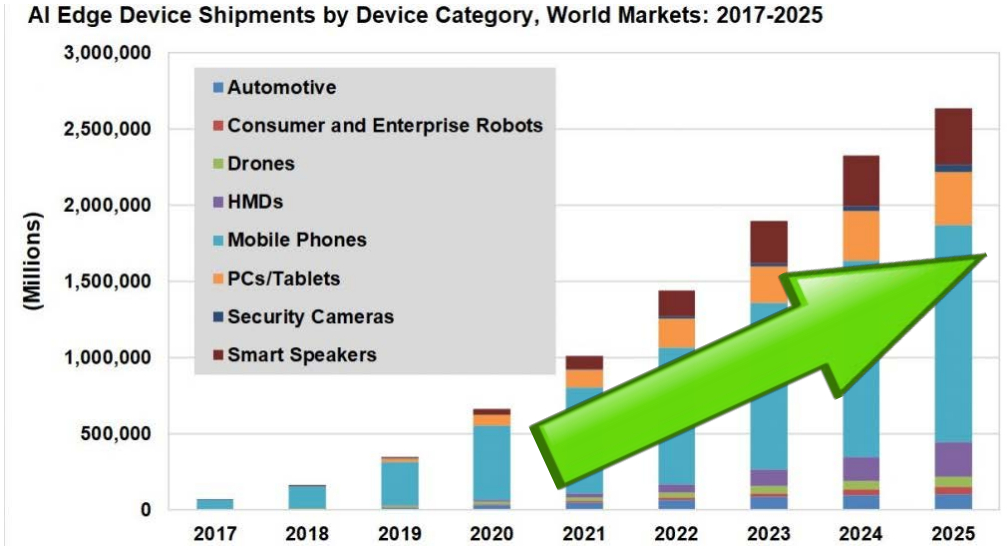
Security and Privacy

Industry key words: AI and 5G

Industry landscape: What trends will drive the industry

AI

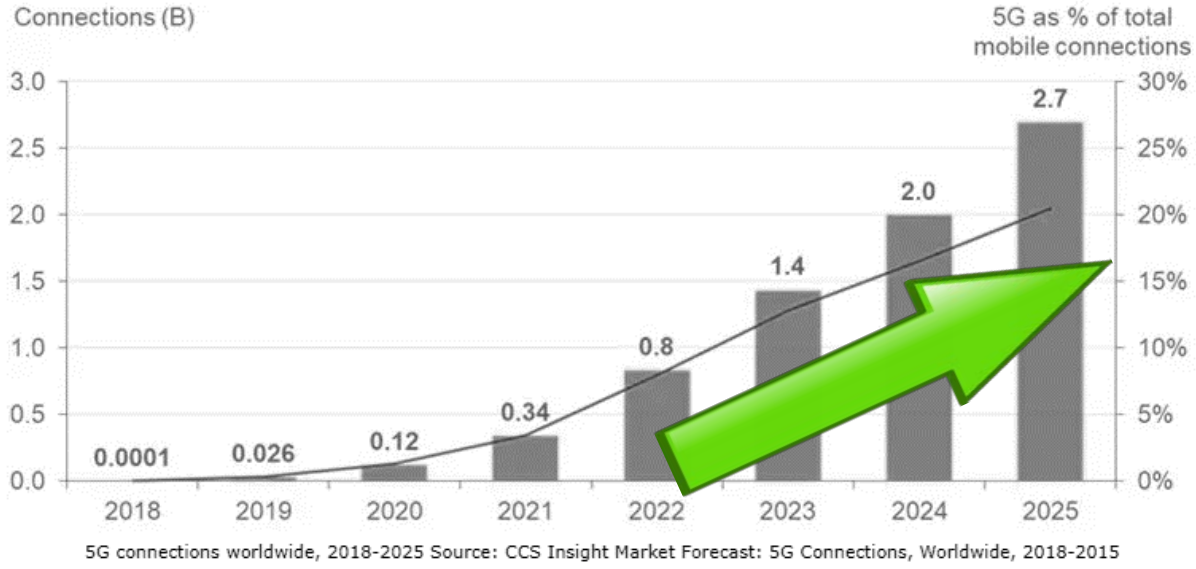
- AI is everywhere!
- AI cuts across applications spaces
- Projected continued growth across all applications



Source : Tractica (2018)

5G

- Still in early phase of deployment
  - Starting with 5G infrastructure
- Initial 5G smartphones from 2019
  - With a slow ramp to follow

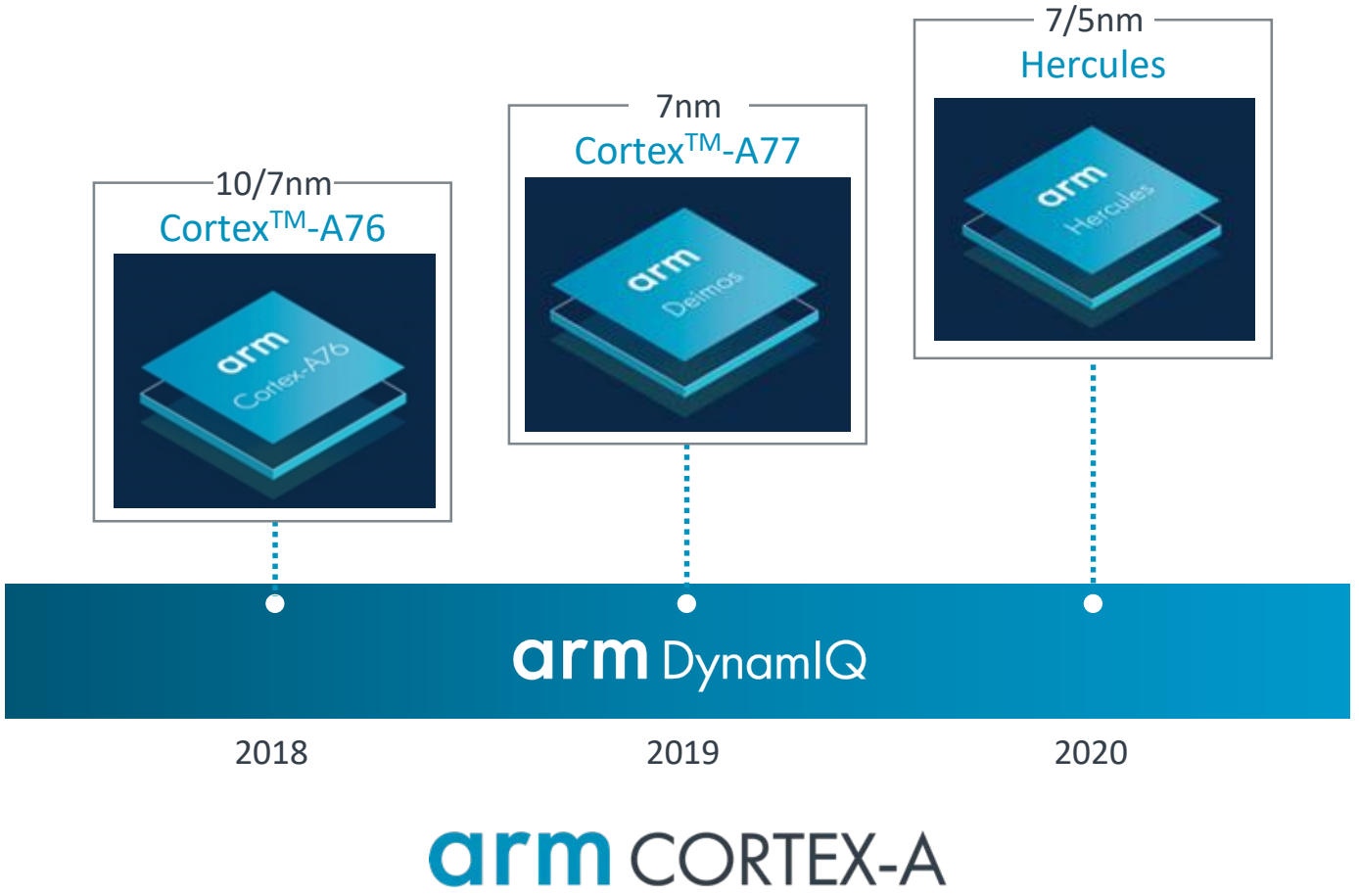


5G connections worldwide, 2018-2025 Source: CCS Insight Market Forecast: 5G Connections, Worldwide, 2018-2015

arm

Breakthrough performance for always-on, always-connected

Continuing the trajectory of increased compute performance for AI, ML and premium mobile

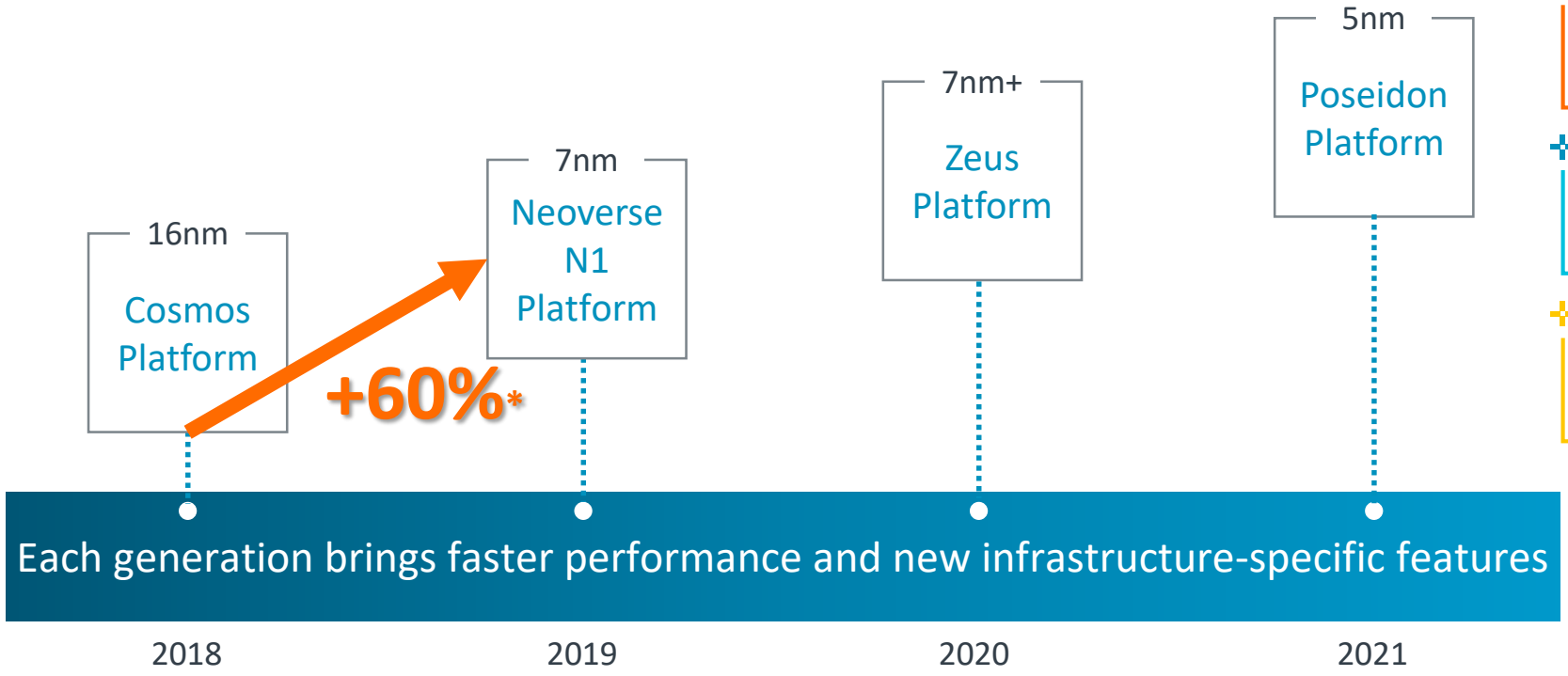


- **Cortex-A76: High Performance Implementation: 3+ GHz in 7nm**
- **Cortex-A77: Up to 20% improved IPC performance**
- **Hercules: Continuing performance and efficiency leadership**
- **Supports the flexibility of Arm® DynamIQ™ big.LITTLE™**

arm

Infrastructure: 5G, cloud to edge foundation

Arm Neoverse™ N1 CPU: Significantly exceeding performance commitments



- **High Performance, Secure IP and Architectures**
- **Diverse Solutions and Ecosystem**
- **Scalable from Hyperscale to the Edge**

arm NEOVERSE

*Spec int 2017 estimate, base, rate=1

arm

Infrastructure: 5G, cloud to edge foundation

Arm Neoverse™ N1 CPU: Significantly exceeding performance commitments

16nm

Cosmos Platform

Each generatio

2018

*Spec int 2017 estimate, base, rate=1

News Release

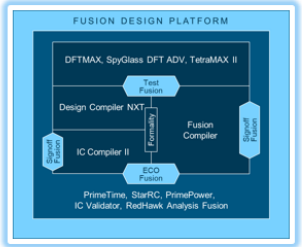
Synopsys and Arm Collaborate to Enable Tapeouts by Early Adopters of Arm's Latest Premium Mobile Processors

Synopsys Design and Verification Platforms and DesignWare Interface IP Enable Optimized PPA and Faster Time-to-Market for Smartphones, Laptops, and Other Mobile Devices

MOUNTAIN VIEW, Calif., May 26, 2019

Highlights:

- Synopsys' Fusion Design Platform enables faster implementation with optimized PPA for Arm processors
- QuickStart Implementation Kit (QIK) using Arm Artisan Physical IP and POP IP, including scripts and reference guide, available today from Synopsys for new Arm Cortex-A77 processor in 7nm process technology
- Tapeout success by early adopters of Arm Cortex-A77 CPU and Mali-G77 GPU
- Synopsys' Verification Continuum Platform accelerates verification closure and quality for Arm-based designs
- DesignWare Interface IP, including controllers and PHY for USB, DDR, PCI Express, MIPI, and mobile storage, enables rapid development of mobile Arm-based SoCs



Synopsys' Fusion Design Platform Enables Successful Tapeouts of Arm's Latest CPU and GPU

Arm + Synopsys Collaborating for 25+ Years

arm

"Building on the previous successes of the Cortex-A76 and the Neoverse N1 platform, early engagement with Synopsys on our new suite of IP has delivered complete solutions to enable the next generation of Arm-based mobile devices.

Ian Smythe
Vice President of Marketing
Client Line of Business

e, Secure IP s

s and

perscale to

VERSE

arm

Translating Arm RTL benefits into silicon

HOW TO

Translate the year-over-year **performance improvements of >15%** for compute through 2020 in silicon

?

Optimize implementation for new cores and advanced process nodes

?

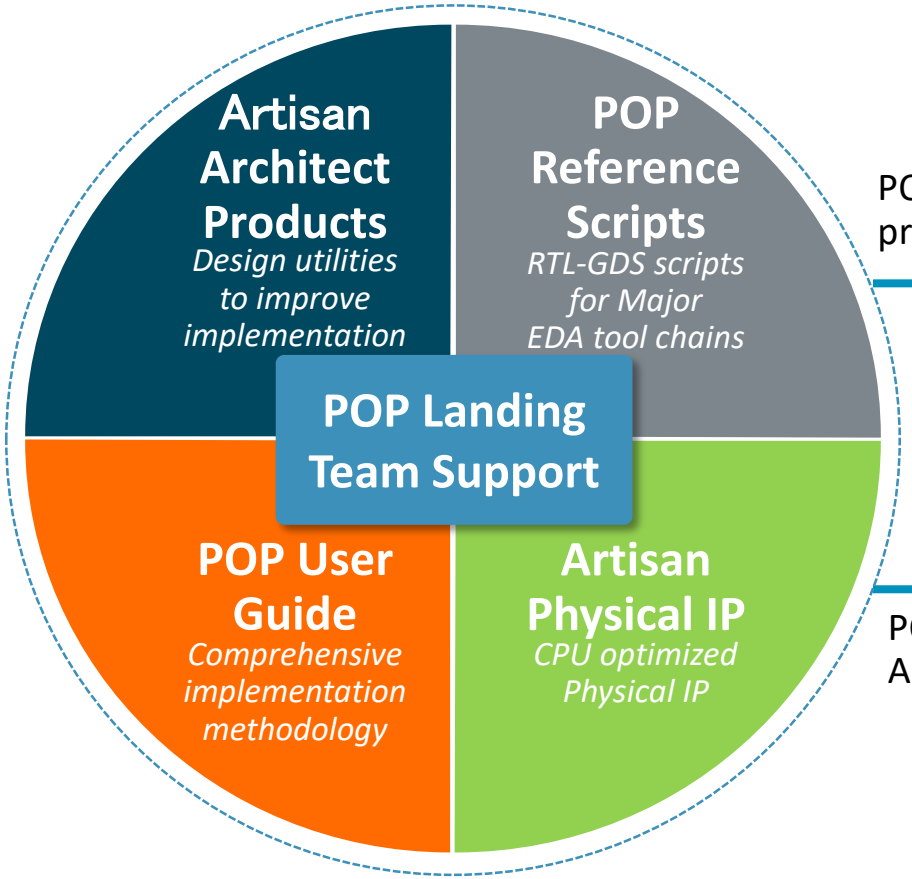
Ensure **fast turn-around time** such that increased productivity of new Arm cores

?

arm

Arm POP IP is optimized Arm core implementation

POP IP Components



POP is available for major foundries producing on 28nm & more advanced nodes

tsmc

and other foundries

POP achieves the best possible PPA for Arm cores

arm NEOVERSE
arm CORTEX-A
arm MALI
arm ARTISAN

Comprehensive support and services

arm

Transforming markets with optimized Arm Physical IP

Mobile and Consumer

- High performance
- Low power
- Cost (area) sensitive
- Flexible performance requirements

Mainstream
- 16/12nm
- 28/22nm

Premium
- 7/5nm

Networking and Servers

- High performance
- Fault tolerance
- Long lifetime
- Continuous operation

Networking
- 7/5nm
- 16nm
- 28/22nm

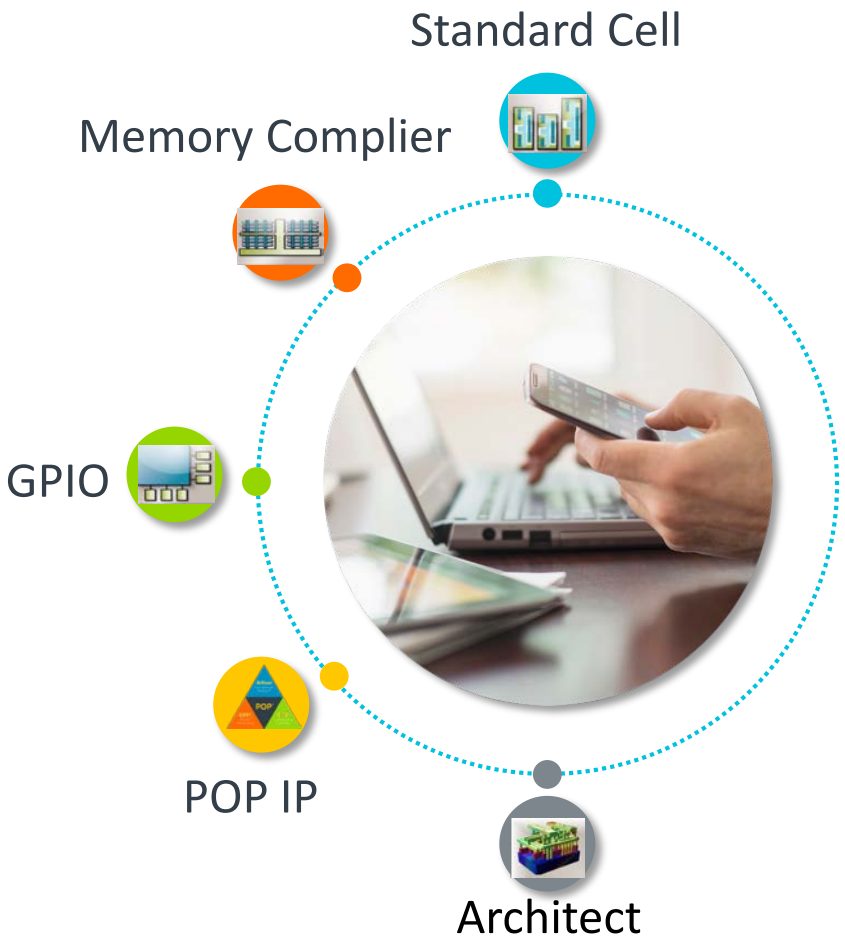
Server
- 7/5nm

arm

Arm Artisan on TSMC 7FF platform

Engineered for Success

- **POP IP** for best-in-class PPA for Cortex-55, Cortex-A75, Cortex-A76 and Neoverse N1
- Optimized **Fast Cache Memory Instances** for highest performance
- Memory IP designed to minimize variation
- **Flexible power grids** to reduce IR drop and improve quality of implementation
- **Small footprint** programmable GPIO



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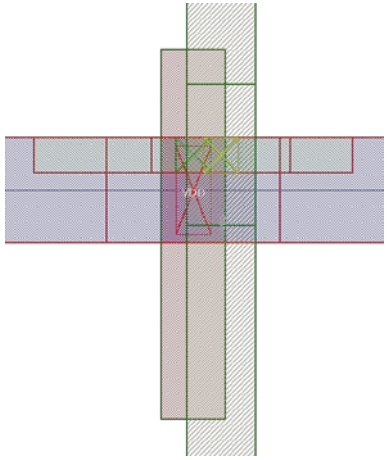
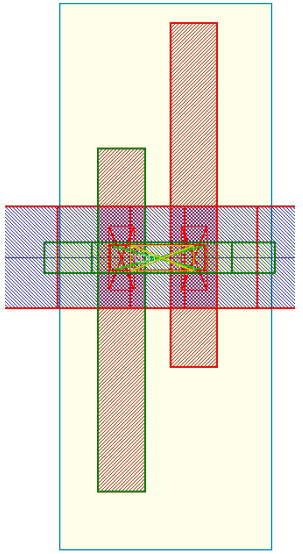
Arm differentiation in logic

M0 input pins	• Allows easy connection from M1/M2 to cell input (M0) pin
Focus on pin-access	• At least two hit-points per pin
Support for multiple colored EEq GDS variants	• Allows closer cell-placement increasing utilization • One common liberty file
Flexible power-grid	• Multiple M1/M2/M3 power-grids options supported to trade-off routing density and EM/IR requirements





arm

Benefits of Arm memory compilers

Design Considerations

Internal routing optimized for 7FF technology overcomes increased via resistivity

Cell-based memory development methodology reduces variation and improves manufacturability

Compile-time features

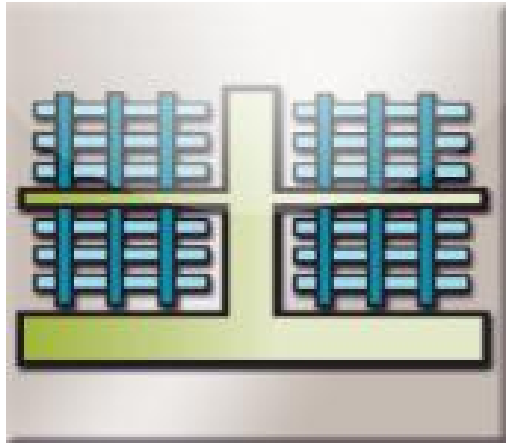
Dual operation mode to trade-off performance and power

Multiple progressive power modes including retention

Full scan on input pins to improve testability for high reliability applications

Post silicon assistance

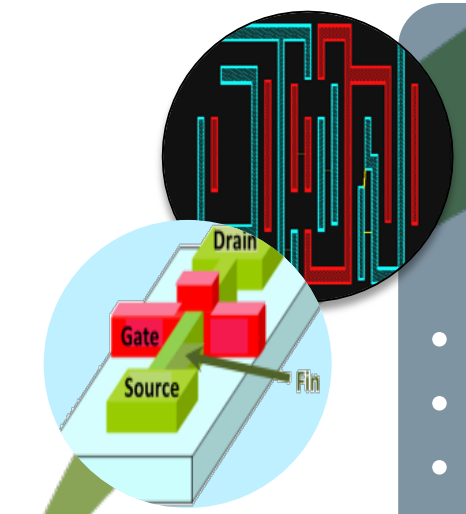
Programmable Extra Margin Adjust pins to tune post-silicon performance



Implementation challenges

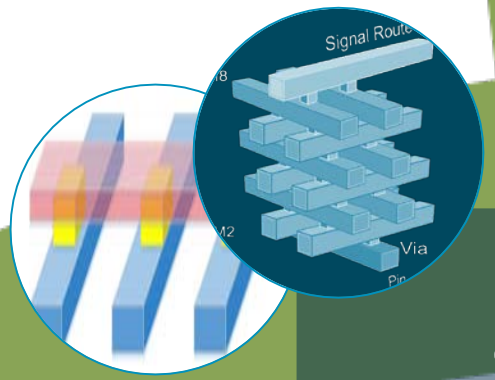
Challenges present for advanced nodes and cores

Advanced nodes



16nm

- FinFETs
- Placement rules
- DPT-aware colorless routing



7nm

- Via ladders
- New placement rules
- Power grid challenges
- Addressing variation

Latest Arm Cores

- Concurrent configuration of CPU with DynamIQ™ Shared Unit (DSU)
- Asynchronous configuration
- Long channels between DSU and CPU slaves
- Private L2 cache
- Architectural clock gating

arm

Arm IP enables designs using Synopsys' Fusion Design Platform™

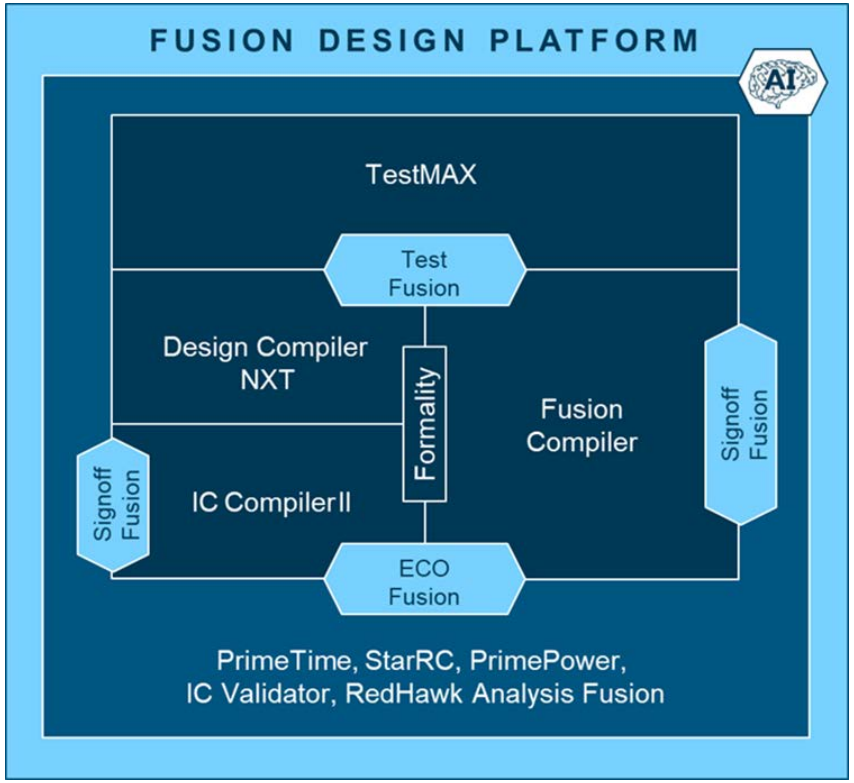
Translate Arm RTL benefits into silicon

Arm POP IP and Artisan physical IP

- Deliverables support Fusion Design Platform …and more

Simulation	VCS
Synthesis	Design Compiler family
Design planning, P&R	ICC, ICCII
STA and SI/noise signoff	PrimeTime
Power Analysis & IR drop signoff	Power Compiler, PrimeTime PX, RedHawk
DFT	TetraMAX, SMS
Power intent	UPF

Fusion Design Platform



arm

Agenda

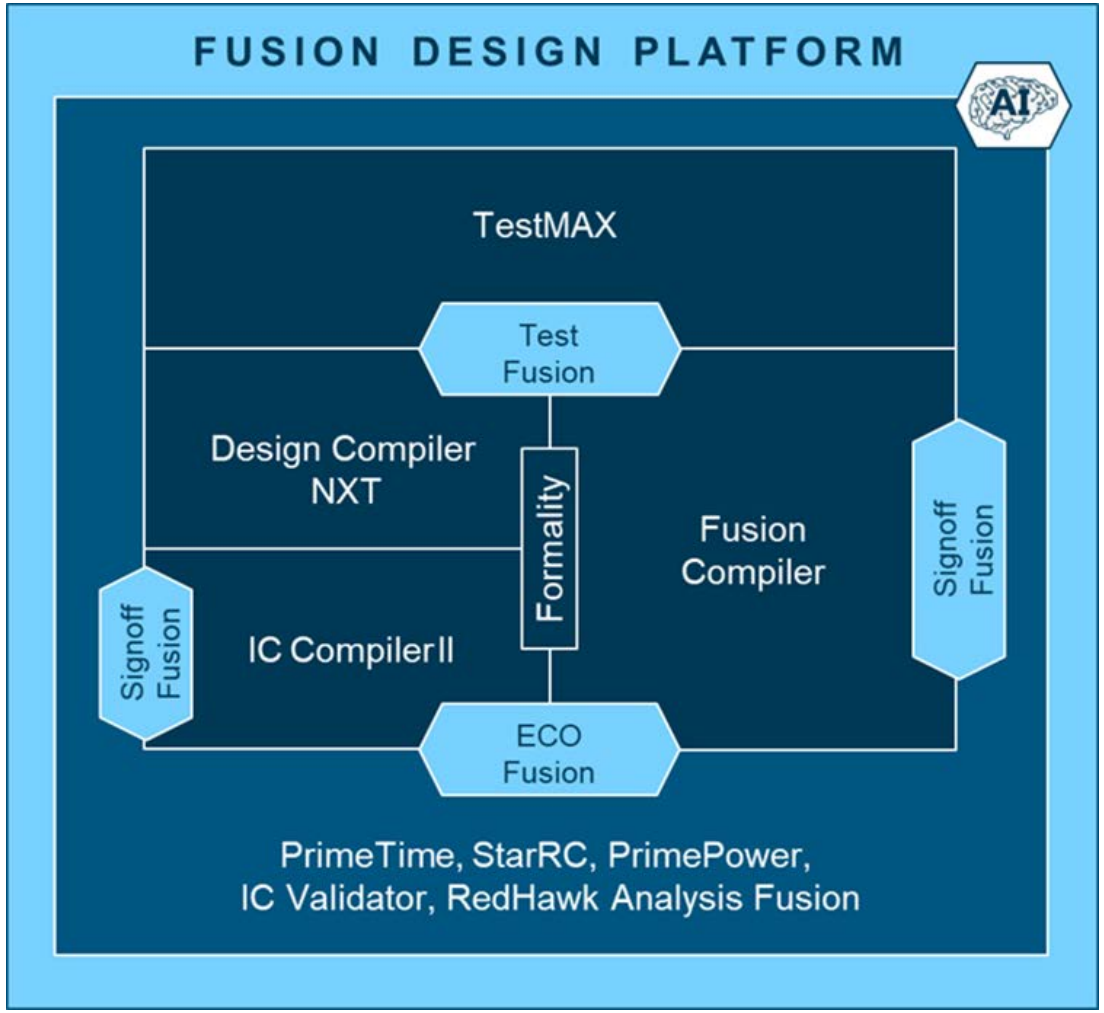
Challenges on the Horizon

Synopsys Fusion Compiler

Deploying Fusion Compiler for Arm CPU

Introducing Fusion Compiler

Architected to Deliver Fastest Convergence and Best QoR



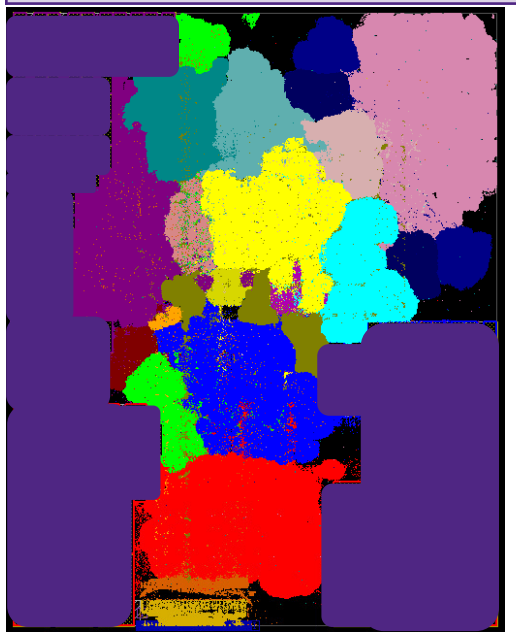
Innovative RTL-to-GDSII product with fusion of Synthesis and Place-and-Route

Unified Data Model, Single Cockpit and Infused Industry Golden Sign-off delivers most Convergent Design Flow Possible

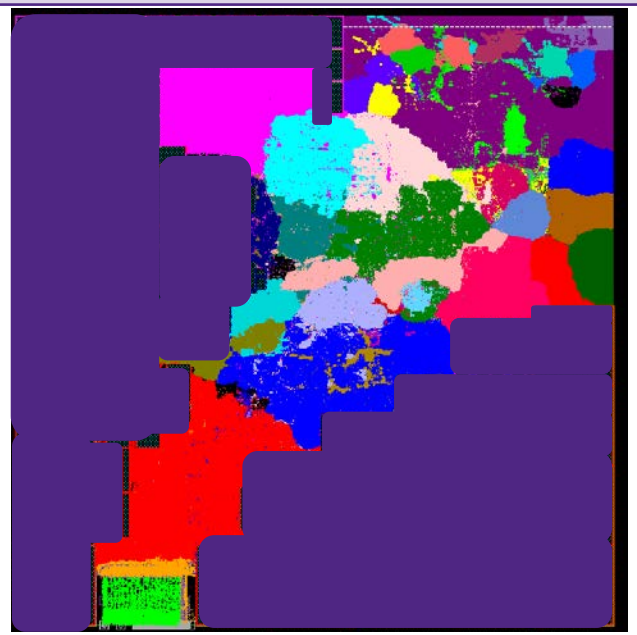
20% Better Quality-of-Results
Faster Convergence and TAT

Fusion Compiler on Arm's Latest Performance-Optimized CPUs

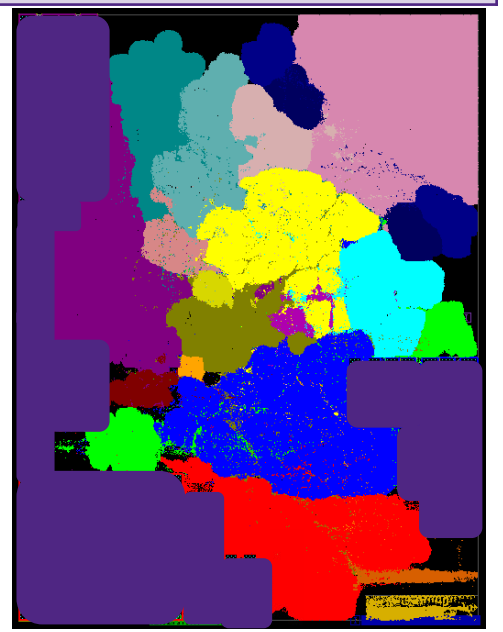
Design Details	
Routing	13 Layer + AP w/ routing on M1-M11
Libraries/ memories	Arm POP IP with Artisan 7nm SVT/LVT/ULVT C11/C8 standard cell libs
PVT corners MCMM	1 or 2 setup corners, power corner, hold corner
DFT Strategy	DFT with scan compression
UPF	3 power domains with level shifters and enable level shifter required



Hercules



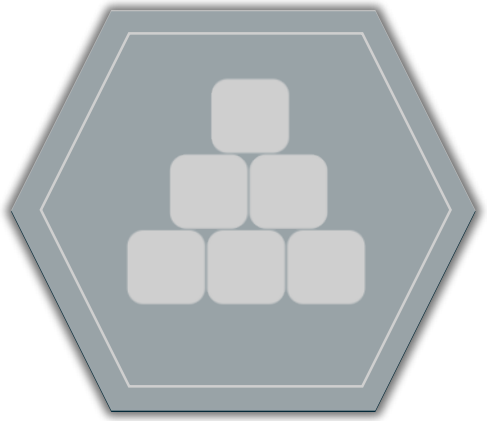
Arm Neoverse N1 CPU



Deimos

Fusion Compiler Highlights

The Fastest and Most Convergent RTL-to-GDSII Design Solution

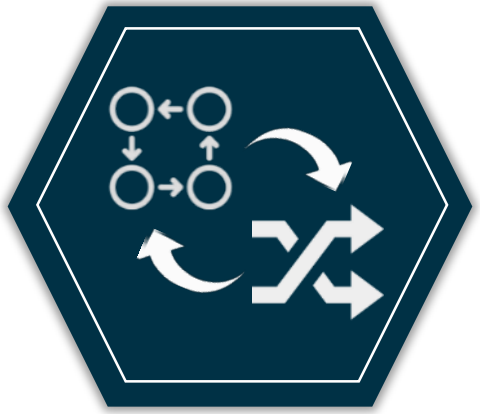


LEADING FOUNDATIONAL TECHNOLOGIES

Ultra-Scalable Data-Model

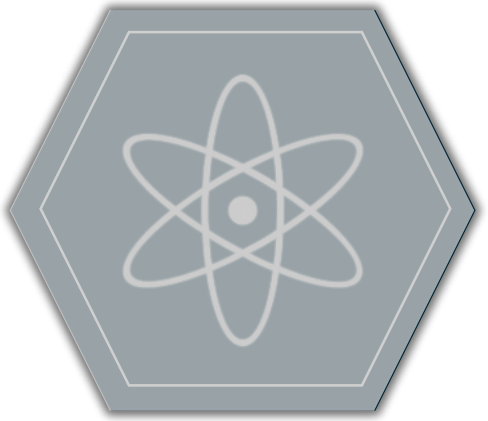
Common Engines

Golden Sign-off Backbone



COMMON OPTIMIZATION

- Reduced logic levels
- New placement technology
- Ram/Register skewing
- CCD everywhere



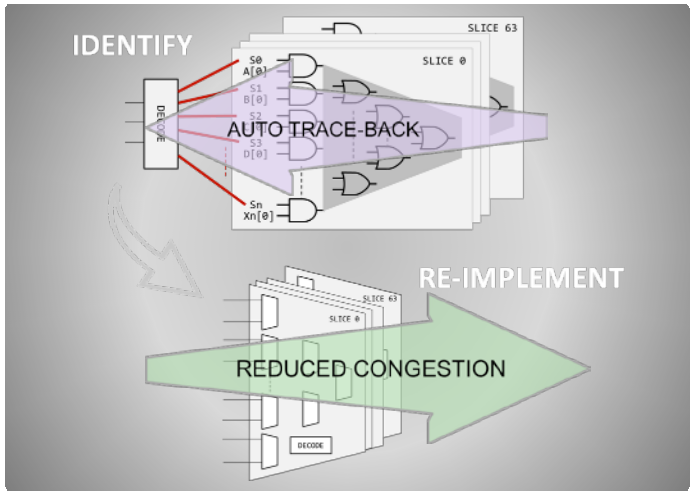
THE FUSION DIFFERENTIATION

Platform-Wide Technology Infusions for OOTB QoR and Productivity:
ECO, Signoff, IR, Test

Deployment of Fast, Novel Synthesis Technologies

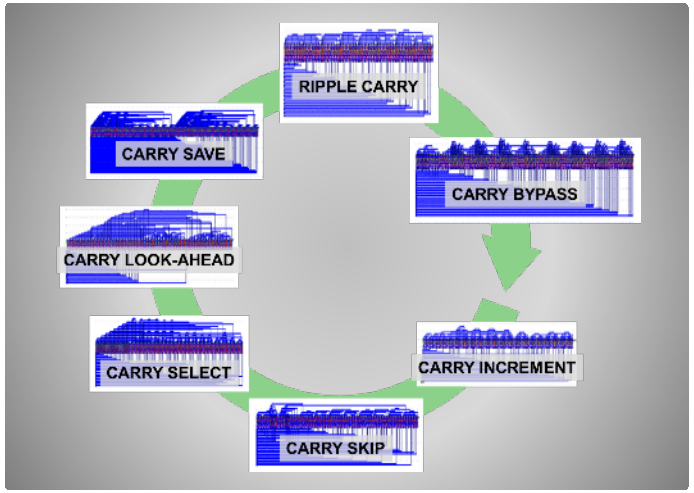
Physically Optimized Synthesis to Deliver Optimum Throughput and Highest PPA

Congestion-Aware Mux Re-synthesis



- Automatically restructures AO-based trees using mux cells
- Defers the decode/recode logic along the mux tree
- Delivers faster TTR and improved DRC convergence

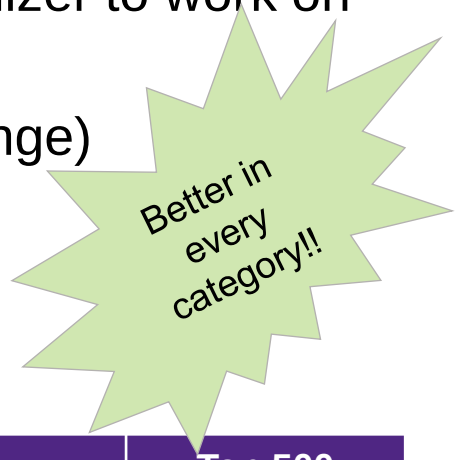
PPA-Aware DesignWare Re-selection



- Post-placement architecture re-selection based on design context
- Delivers optimum PPA

Technologies to Reduce Logic Depth of Complex Datapath

- Map to speed from elaborate and “preserve” through flow
- Intentional skew on multiplier sum registers
- Intelligent path groups created on sub-hierarchies of VX multiplier– allow optimizer to work on overlapping paths to final SUM registers
- Logic level costing prototype in FC RTL Synthesis (wns gain vs logic level change)
- Additional compile directives for Arm critical RTL modules
  - infer muxops, 1-bit adders, use wide cells



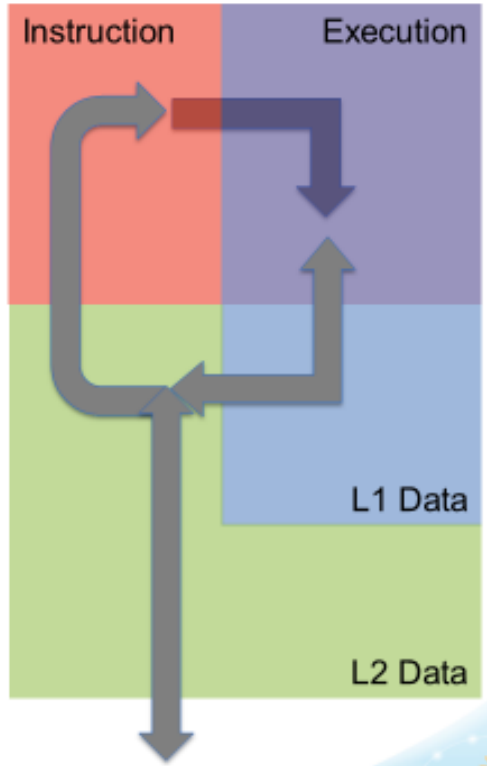
Block Level Testcase	Run Time	Inst CNT	Area	WNS	TNS	% long paths	Top 500 Paths
Baseline	2:52	572k	89932	-28p	-10335n	19.86	20.60
New	3:13	537k	85773	-1p	-61n	18.26	17.61

Arm Core-Specific Placement Challenges

Sub-module Data Flow

Use DFA to Identify Data Flow & Guide Placement to Get Best FMAX

- For absolute best FMAX look into processor data flow
  - OOTB placement is good, but can be further tuned
  - Guide module placement to better align with expected data flow
- Use ICC II Data Flow Analysis (DFA) to visualize connectivity
  - Infer relative locations of cell groups with respect to RAMs and main functional modules
    - Memory-aligned sequential groups
    - Floating Point Unit (FPU) sub-modules
    - Instruction Execution pipeline
    - L1 Data Load and Store registers



SNUG 2018

51

Presented at SNUG 2018

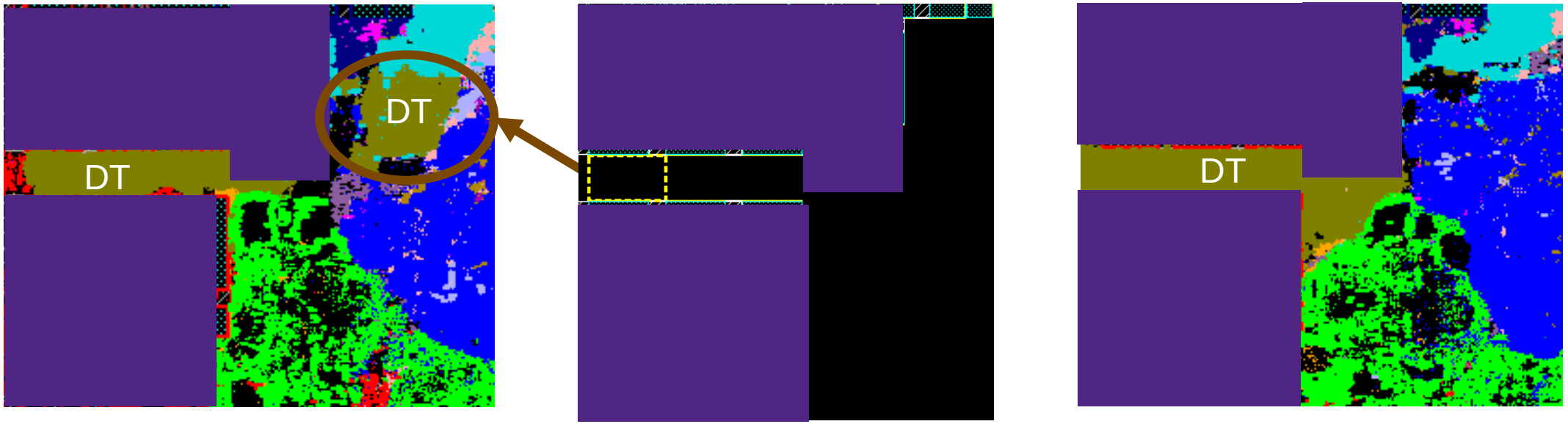
Low Effort Bounds

Guiding Placement of Non-critical Logic

Non-critical debug logic being pulled into channel

Soft Bound used to locate debug logic

Non-critical debug logic placed out of the channel

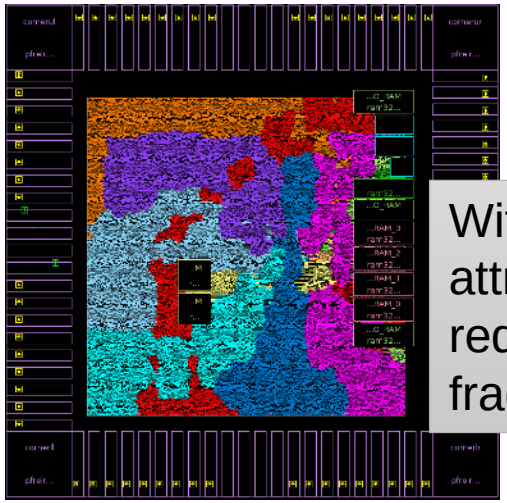



```
set DEBUG [filter_collection [get_cells -hier -filter "is_hierarchical == false"] "full_name =~ *DT*/*"]

create_bound -name DT_bound -type soft -boundary {{180.8 526.2} {242.1 562.8}} [get_cells $ DEBUG] -effort low
```

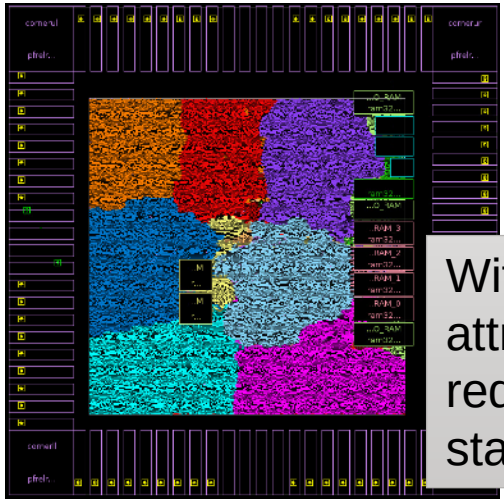
New Technology For Guiding Placement

Placement Attractions, Available in 2019

- A new placement constraint that allows the user to tell the placer where groups of cells should be in respect to each other or a location
- Allows the user to have more particular control over general placement location
- Allows the user to prevent fragmentation of modules



Without attractions, red module is fragmented



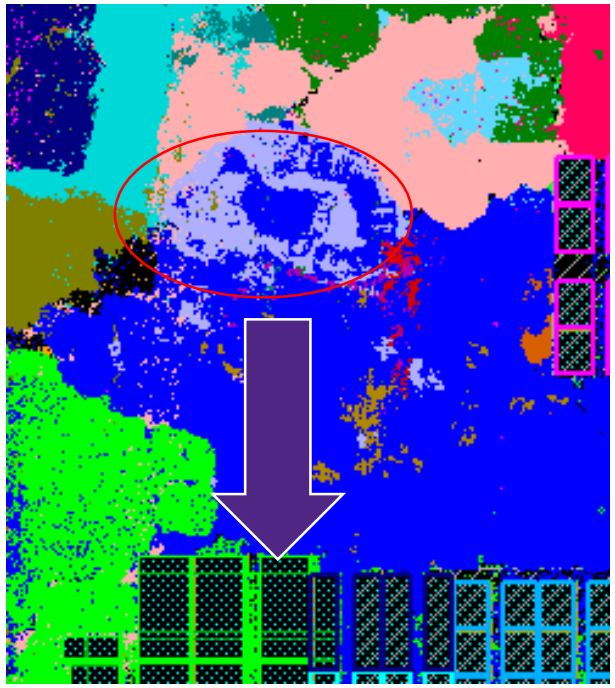
With attractions, red module stays together

Commands	Description
create_placement_attraction	Advise coarse placer on relative placement of modules
remove_placement_attraction	Removes placement attractions
add_to_placement_attraction	Assigns cells to a placement attraction
remove_from_placement_attraction	Unassigns cells from a placement attraction
get_placement_attractions	Find and return existing placement attraction objects
report_placement_attractions	Reports placement attractions

Placement Attractions on Arm CPU

Guiding Placement of Logic to Anchor Point

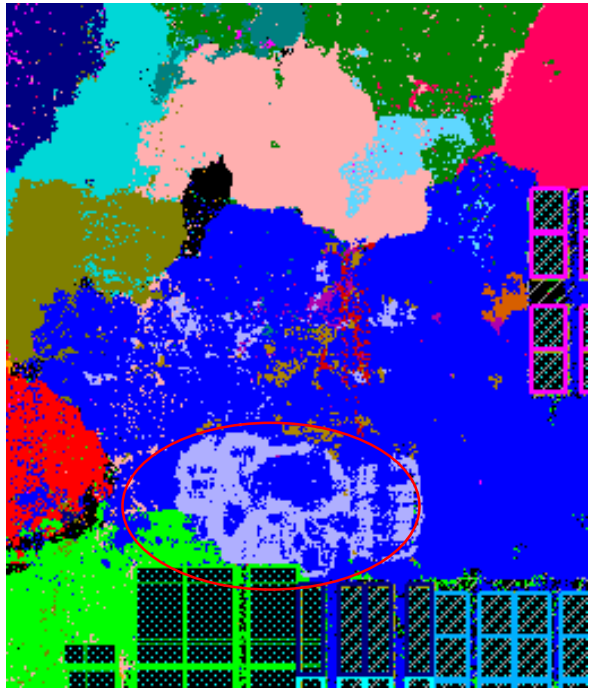
Critical RAM interface logic being pulled into channel



create_placement_attraction between RAM and logical module

```
set abc_cells [get_flat_cells u_abc/*]

set abc_rams [get_flat_cells u_ram/* \
-filter "is_hard_macro==true"]

set ram_mask [create_geo_mask $abc_rams]

create_placement_attraction -name abc_near_ram \
-region [get_attribute $ram_mask bbox] $abc_cells
```

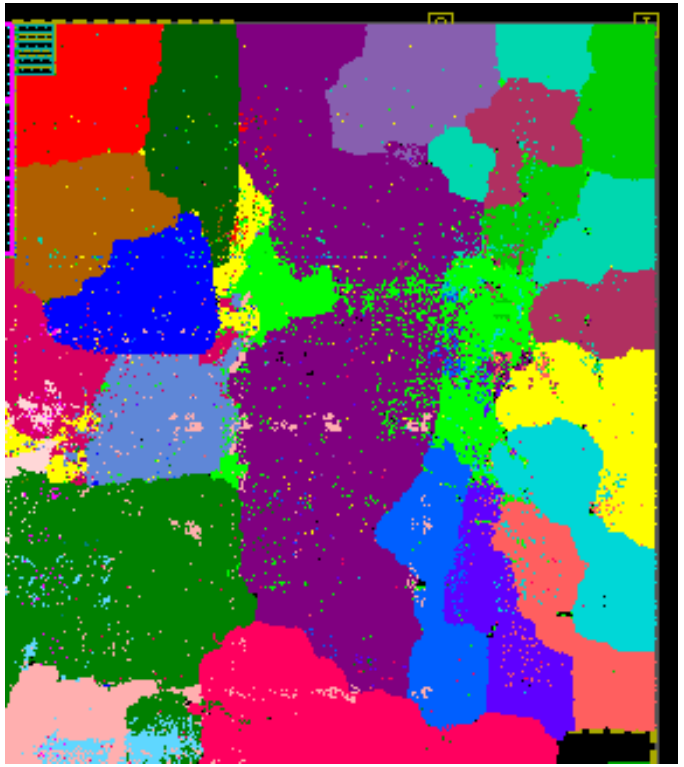
Critical RAM interface logic now held closer to RAM



Placement Attractions on Arm CPU

Guiding Relational Placement of Critical Logic

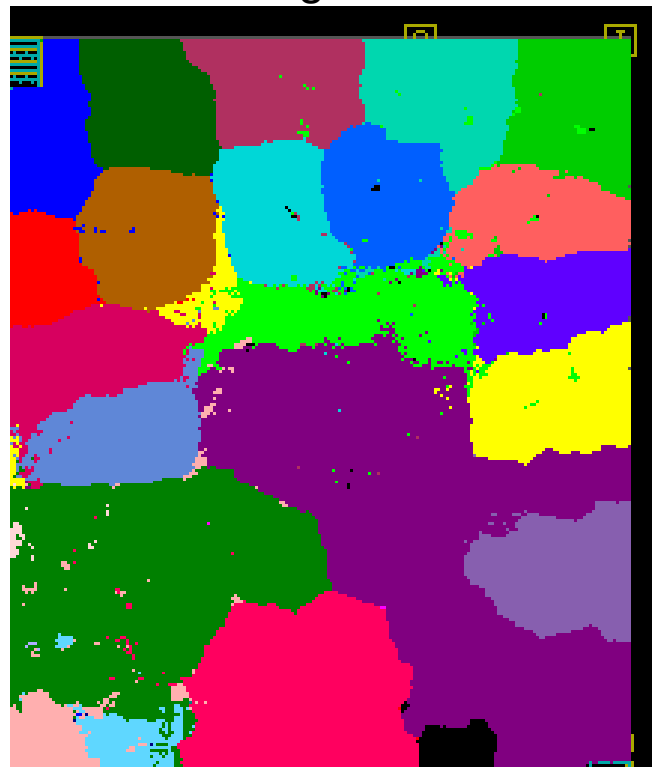
Default placement of complex arithmetic logic



Define placement attraction to hold modules together and relate them

```
set abc_cells [get_flat_cells u_add/u_abc/*]

set xyz_cells [get_flat_cells u_add/u_xyz/*]

create_placement_attraction  -name abc_xyz  \
"$abc_cells $xyz_cells“

set all_add [get_flat_cells u_add/*]

create_placement_attraction -name all_add \
-effort low $all_add
```

Critical modules are held together and relationship between modules more regular

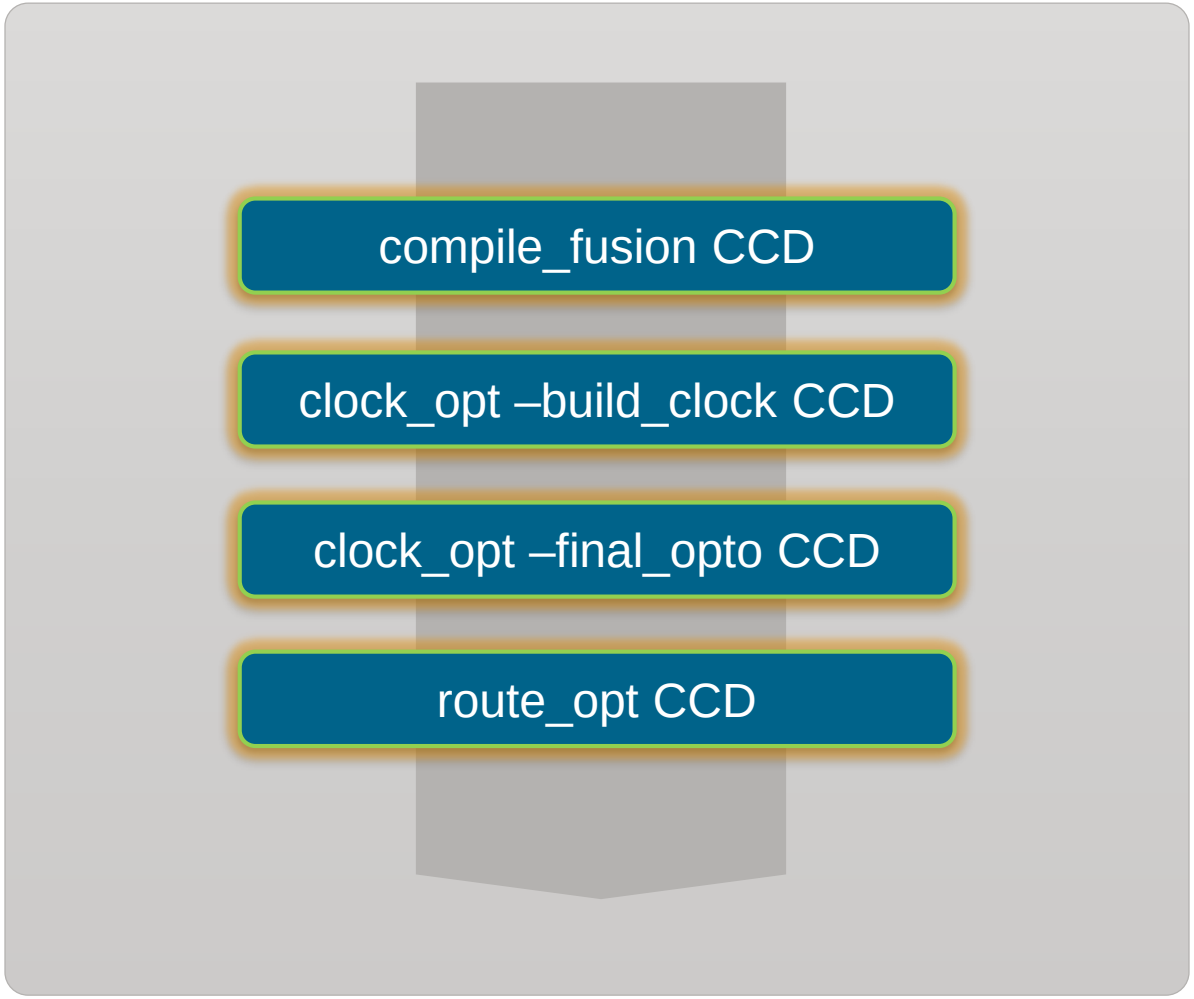


Benefits of Placement Attractions on Arm CPU Flows

- Placement of critical logic less sensitive to changes in the RTL or Floorplans
- Creation of placement attractions simplified
  - Exact size/shape not required
- "Bound management" is not required
  - Placement attractions can stay in place thru entire flow
  - Logic that needs to move to meet critical timing has the freedom to do so
- Placement attractions can be used starting at initial synthesis thru route_opt
- **Placement attractions for Arm cores set automatically**

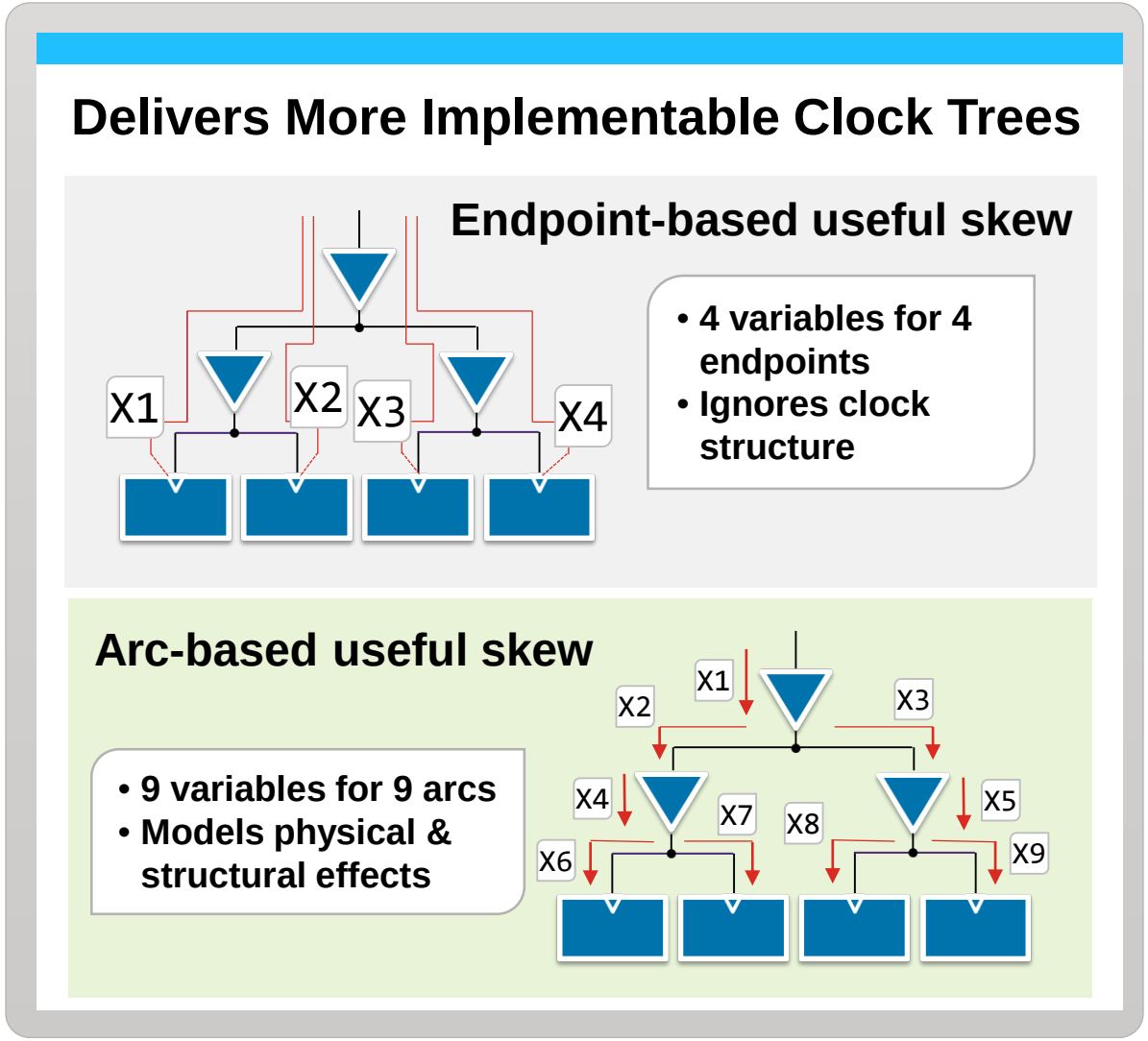
Metric	Baseline	With Placement Attractions	% improvement after place_opt
WNS	-0.123	-0.083	32%
TNS	-296.3	-251.6	15%
NVP	22488	21157	5%

Optimize Timing and Power with CCD Everywhere

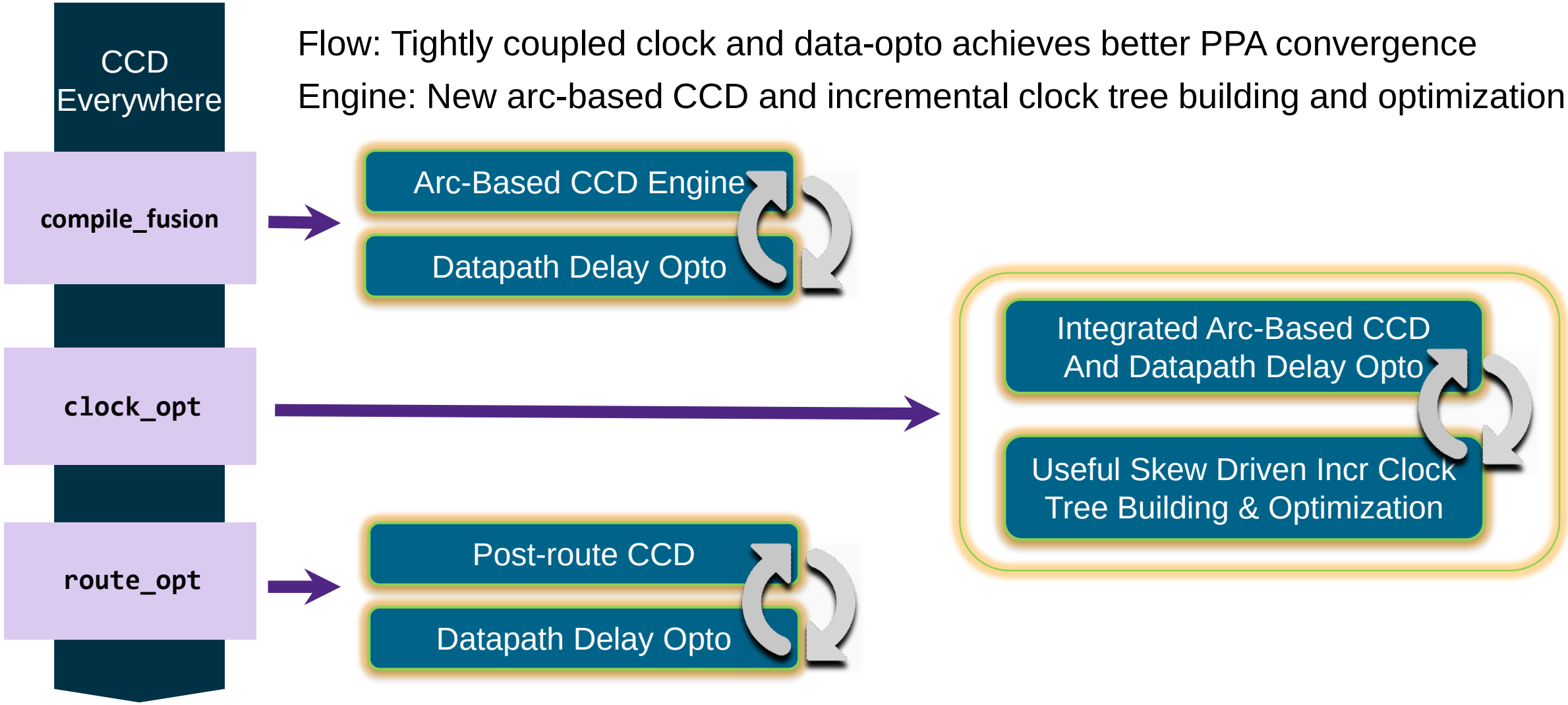


Improved Clock Trees with Arc-Based Global-CCD Engine

- What…
  - Useful skew variables are modeled on delay segments instead of clock end points
  - Clock structural information is directly modeled in the problem formulation and solved naturally with CG solver
- Why…
  - Easier to implement
    - Each arc variable can have its own implementable delay range, coming directly from CTS core engines
  - Better power/timing tradeoff
    - Solver can minimize sum of arc delay changed, corresponding to clock power
  - Better hand-shaking with core CTS engines
    - Support feedback loop from CTS engines, and incrementally refine solution



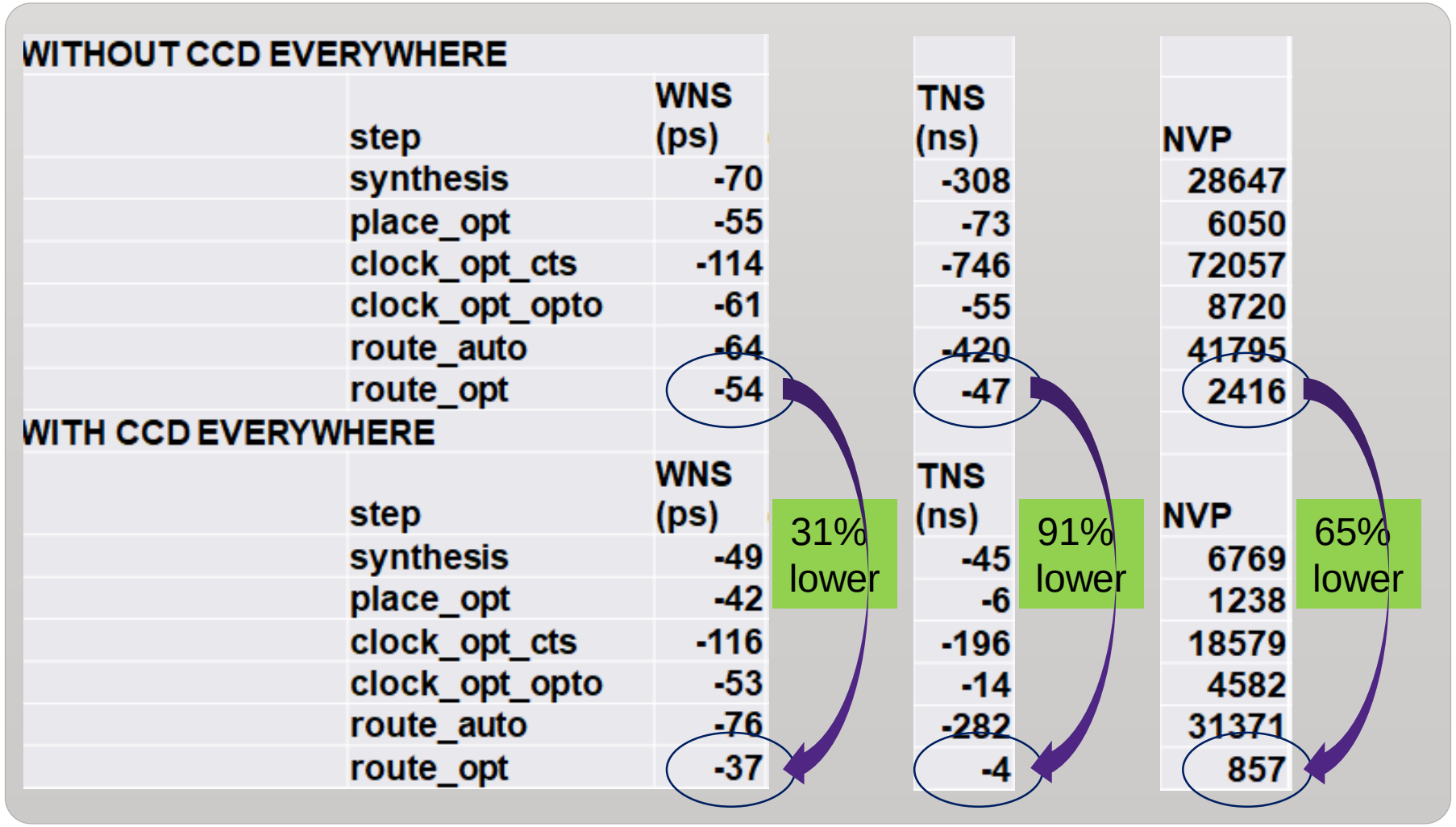
Optimize Timing and Power with CCD Everywhere



Flow: Tightly coupled clock and data-opto achieves better PPA convergence

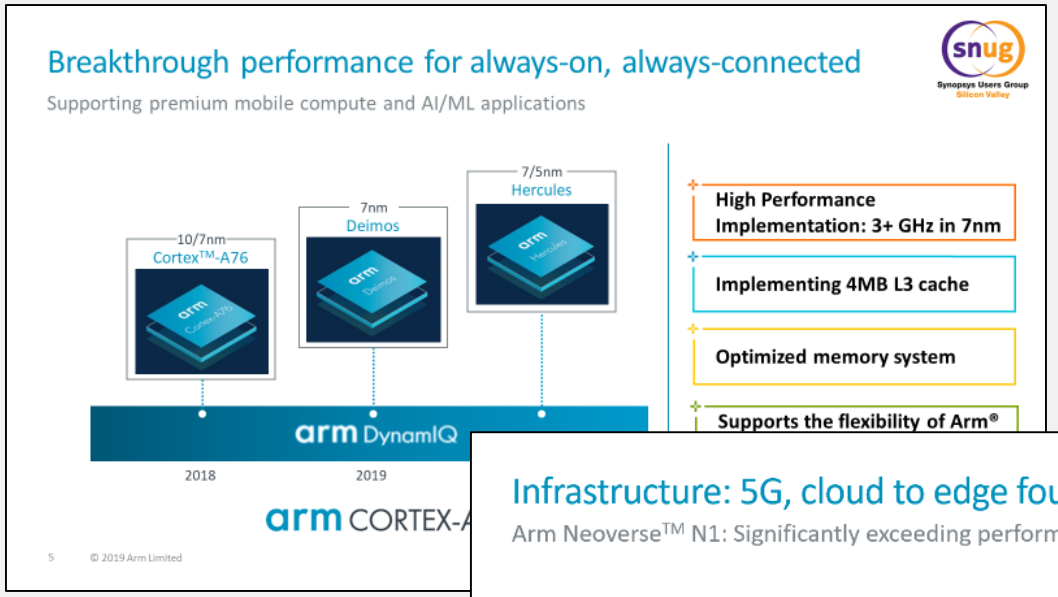
Engine: New arc-based CCD and incremental clock tree building and optimization

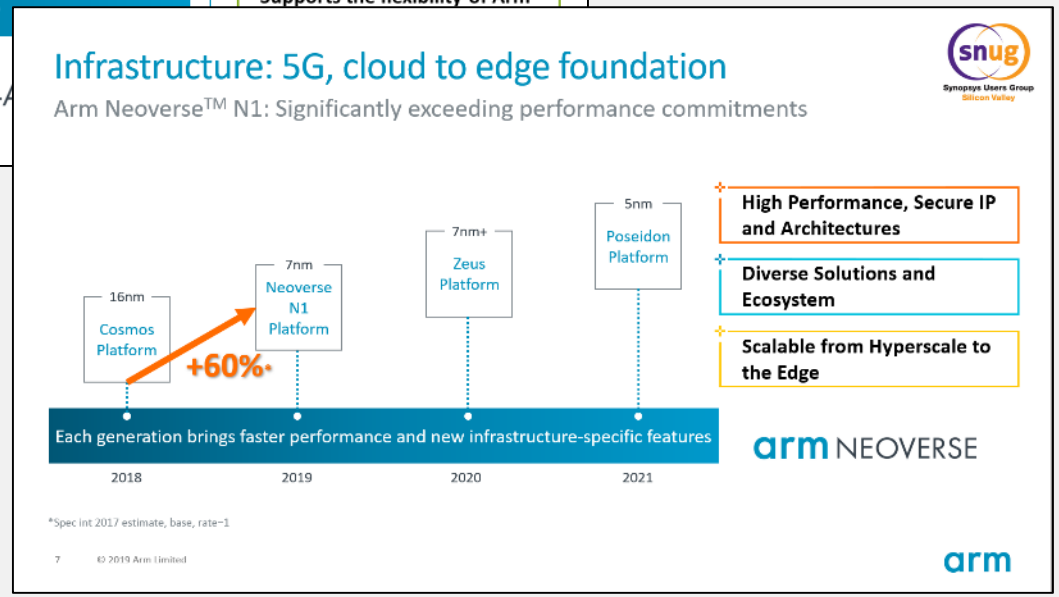
CCD Everywhere Results



- 11% lower leakage
- 2% lower utilization
- Similar runtime
- Similar area
- Similar utilization

Arm Roadmap Demanding More from Collaboration





NEW

Synopsys Fusion Compiler

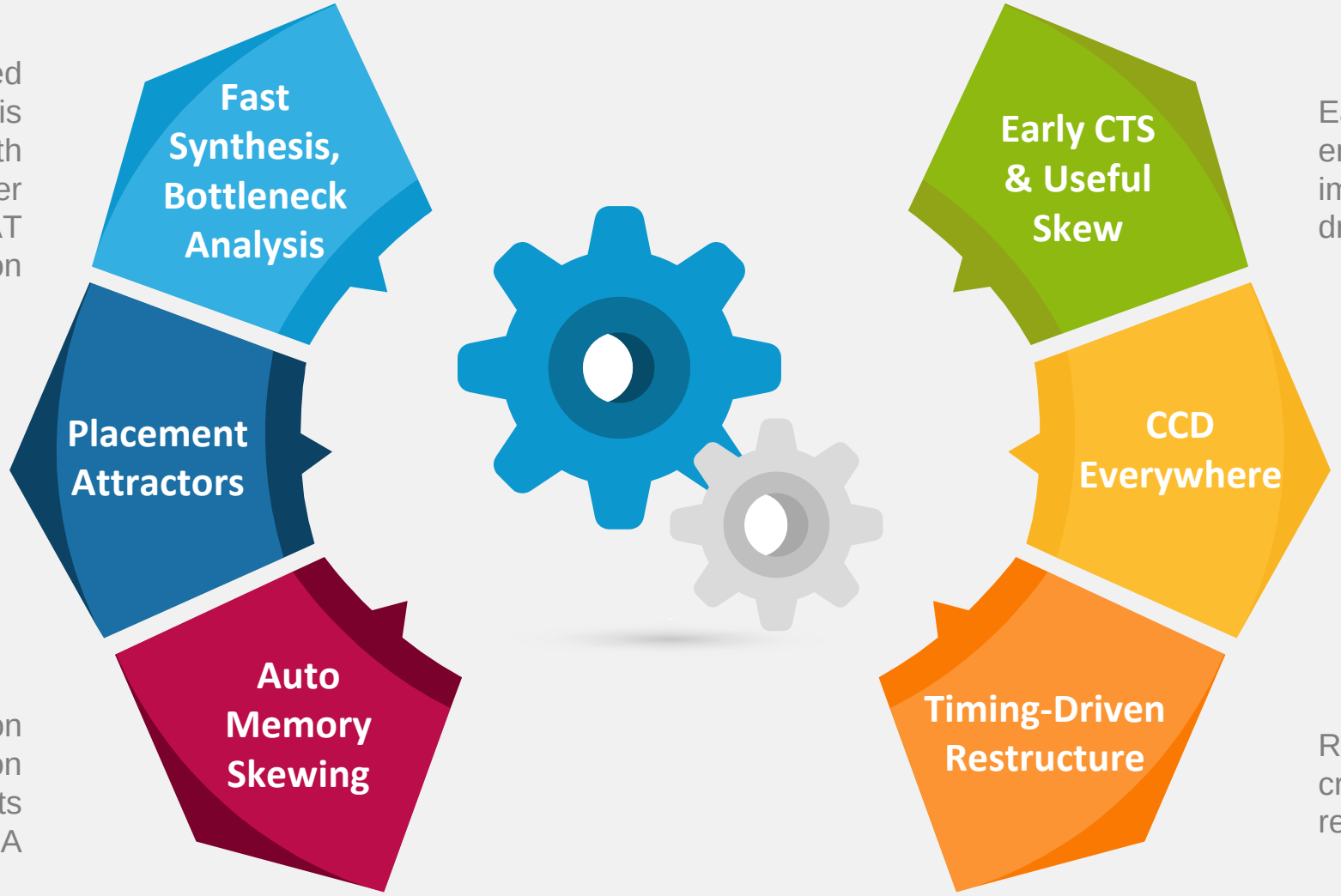
Industry's Only RTL-to-GDSII Solution

Fusion Compiler Collaboration Technologies

Solver-based bottleneck analysis coupled with significantly faster synthesis TAT for exploration

Decouple hard placement bounds from physical floorplans

Optimal calculation and implementation of target-skew offsets to meet highest PPA



Early view of register enable-timing implementability to drive placement

Understand critical pipeline timing dependencies to drive architecture optimization

Re-optimization of critical paths to reduce logic depth

Agenda

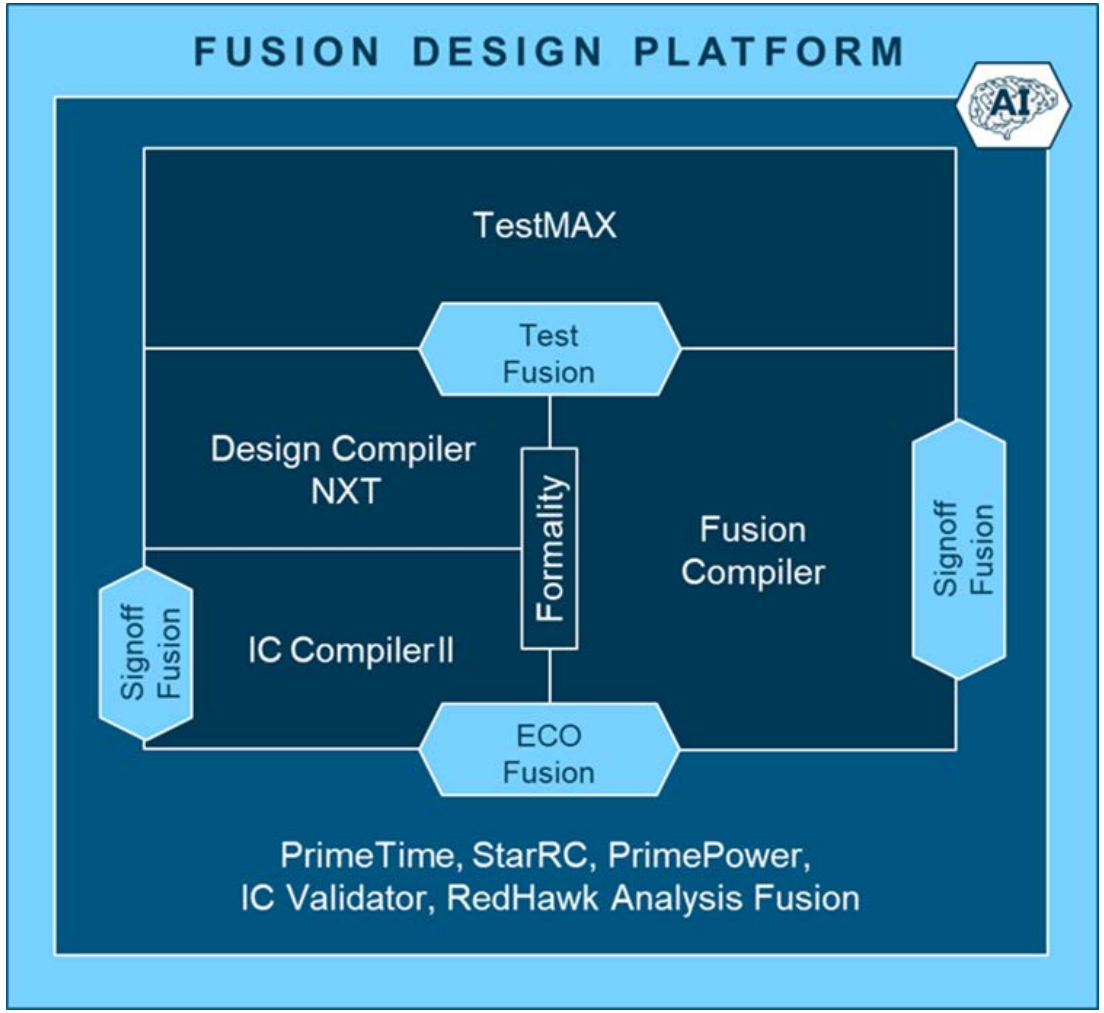
Challenges on the Horizon

Synopsys Fusion Compiler

Deploying Fusion Compiler for Arm CPU

Synopsys QIK

Complete Implementation & Static Verification Flow for Advanced Arm Processors

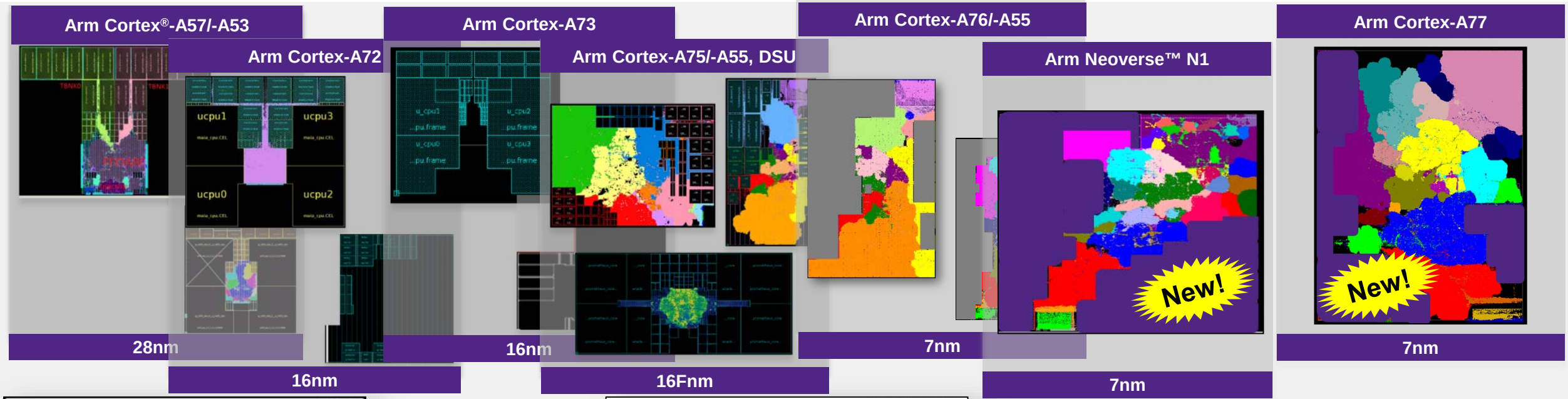


- Recommended flow with scripts
  - Implementation, ECO, signoff, formal verification
- Flat flow for CPU
- Hierarchical flow for sub-system

- Presentation/cookbooks
- Support for 7nm and below

QIKs for Advanced Arm® Cores

Synopsys Reference Flows and Guides to Meet PPA Targets using Arm Artisan® IP



QIKs available to Arm-Synopsys customers, go to www.synopsys.com/Arm

QIKs + Fusion Design Platform

Flexible and Complete implementation & static verification flows

Utilizing the most advanced technologies available in

Synopsys Fusion Compiler

Providing optimal PPA on Arm's advanced processors with Arm Artisan IP

arm + SYNOPSYS®

Collaborating more than 25 years to benefit our customers