Accelerate Power Integrity Closure with RedHawk™ Fusion on the Latest Armv8-A Processors

Arm TechCon 2019

Annapoorna Krishnaswamy, Product Marketing Manager, ANSYS
Rahul Deokar, Product Marketing Director, Synopsys

Sep 2019

arm TechCon

Agenda

- Advanced FinFET Trends and Challenges
- Benefits of RedHawk-SC Technology
- RedHawk Fusion - Shift Left with Power Integrity
  - Robust optimization capabilities within ICCII/Fusion Compiler
- Customer Results
- Summary

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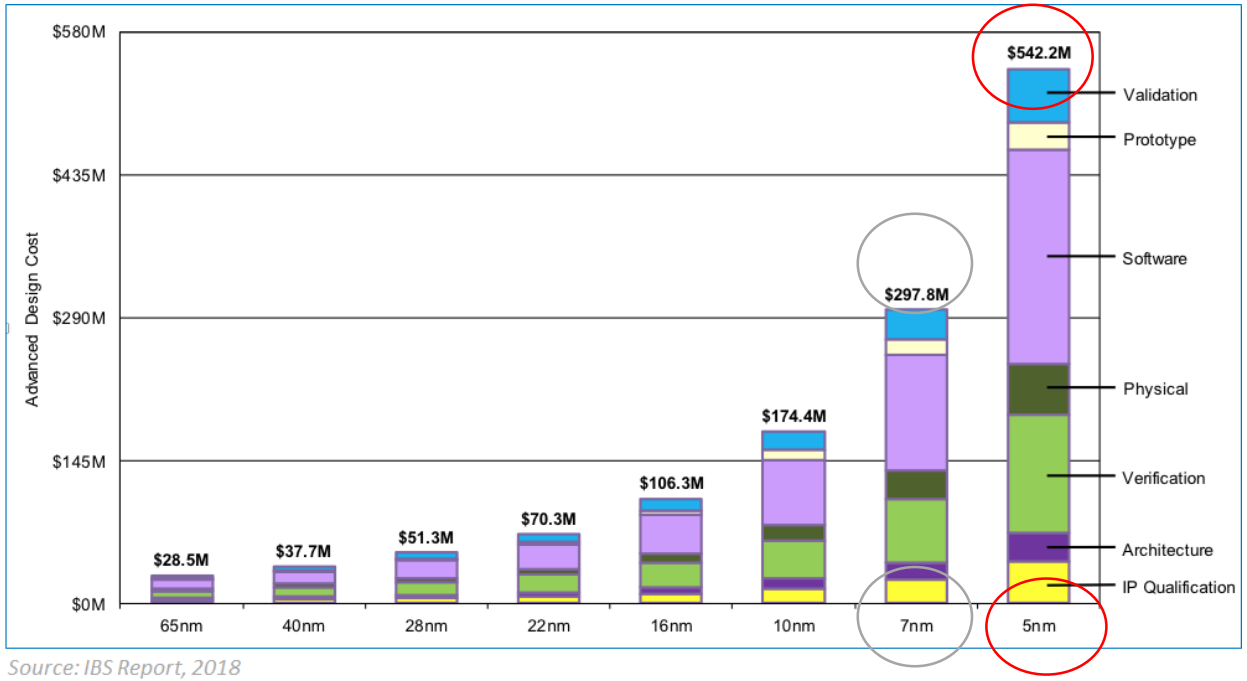
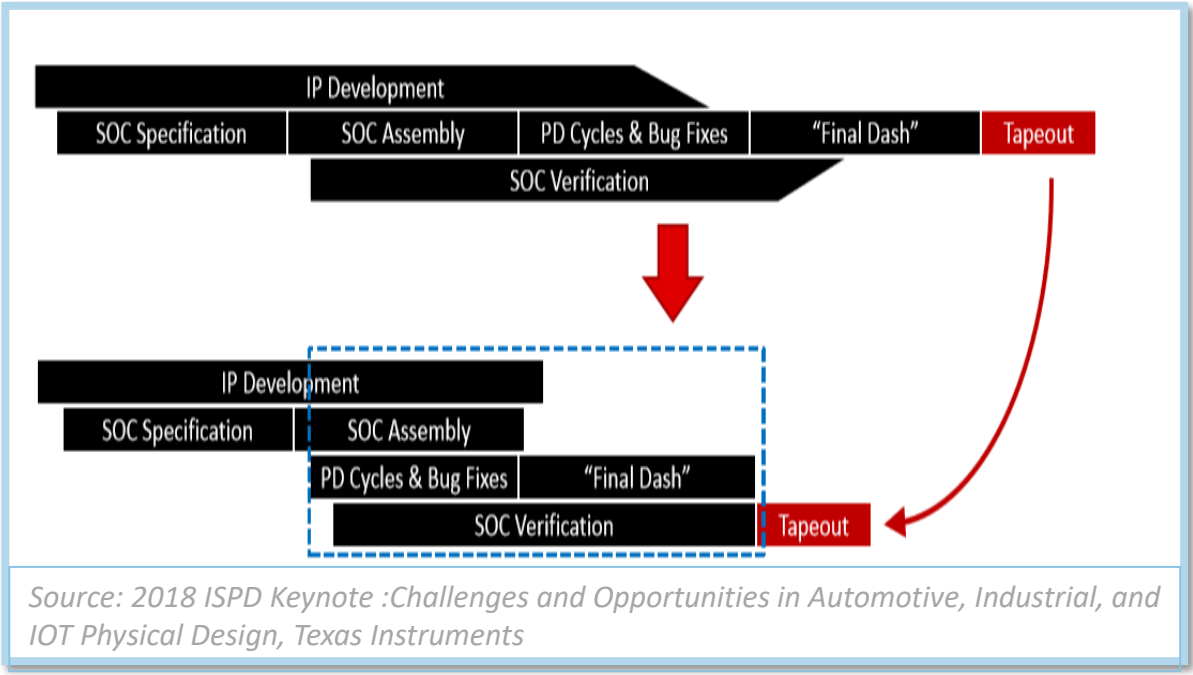
Advanced FinFET Design Trends



Source: IBS Report, 2018



Source: 2018 ISPD Keynote :Challenges and Opportunities in Automotive, Industrial, and IOT Physical Design, Texas Instruments

- **New product design implementation for advanced node takes longer time**
- **But … time to market window is shrinking due to rapidly evolving market requirements**
- **Design cycle time is getting squeezed**
  - Physical design cycle is overlapping IP development, SoC assembly and verification
  - Designers need to work with dirty data and iterate more – **time to results is critical !**

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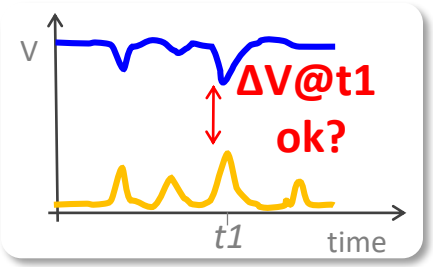
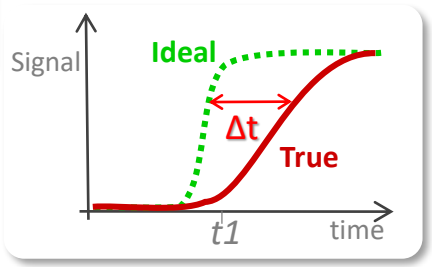
Advanced Technology Related Challenges

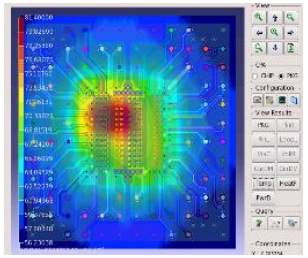
FinFET Power Integrity & Reliability

DvD impacts performance



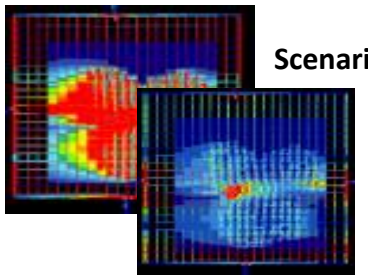


Thermal-Aware Electromigration(EM)

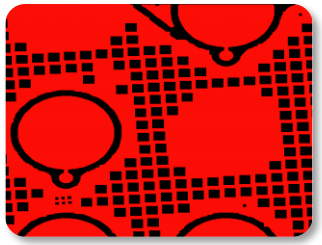


Scenario #1

Scenario #2

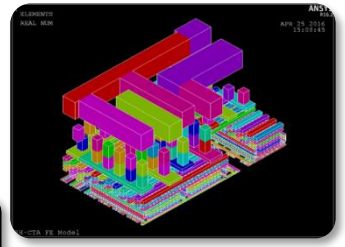


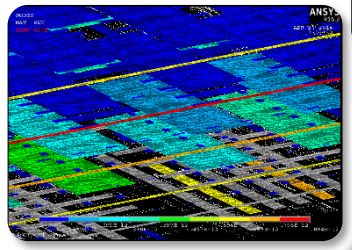
Heterogeneous Packaging (3D-IC)



Complex Routing

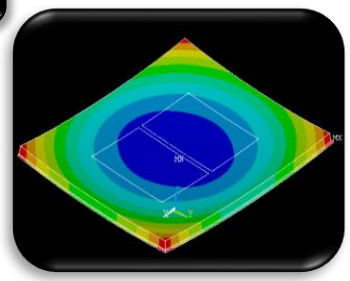
Chip + Package Interconnects



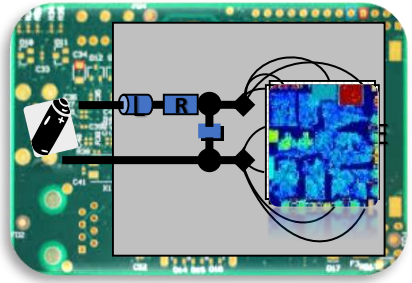


Joule Heating

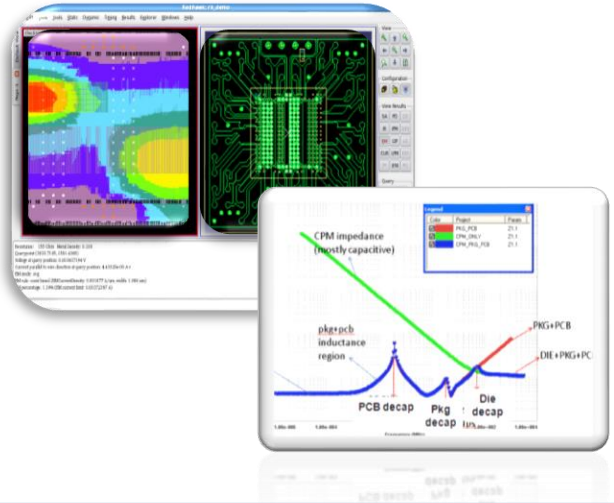
Warpage



Power-Delivery Network Optimization



Chip-Package noise Coupling



Multiphysics and Multiscale Signoff are Critical for Electronics Systems

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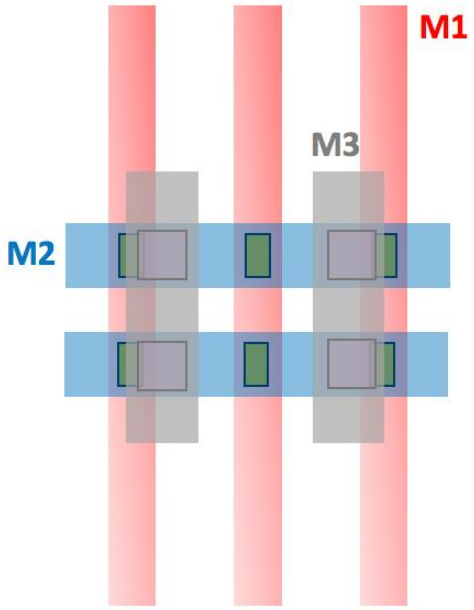
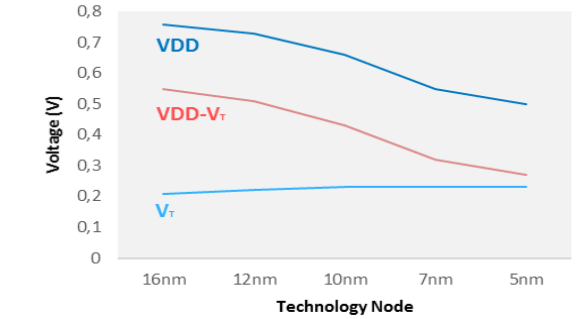
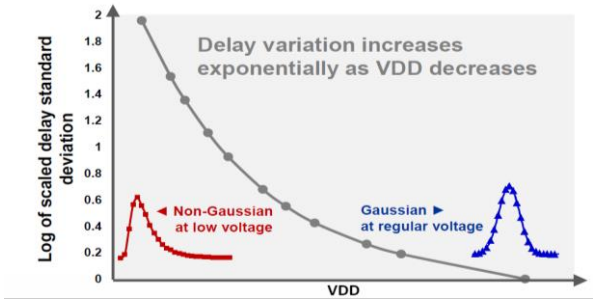
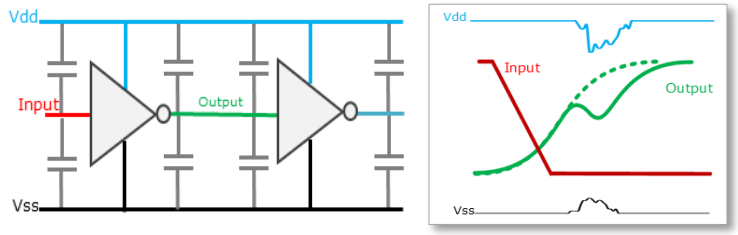
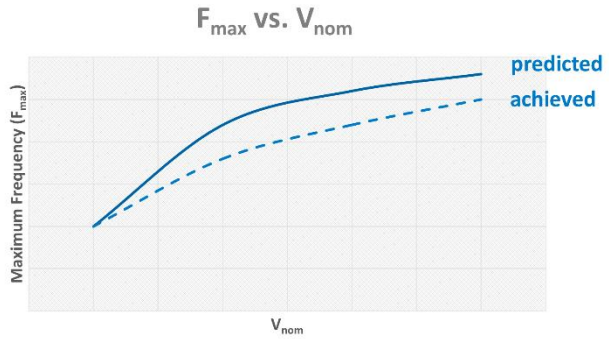
7nm Power Integrity Challenges











5x

Increase in grid complexity, compared to 16nm. Power grids have 10B+ nodes

500mV

Ultra low voltage computing means margins are razor thin, and variability is severe

10x

Need for increased scenario coverage, to ensure voltage and timing

Sources: ANSYS, Paolo Gargini, ITRS Past, Present and Future, TSMC: Physical Design Challenges and Innovations, ISPD 2017

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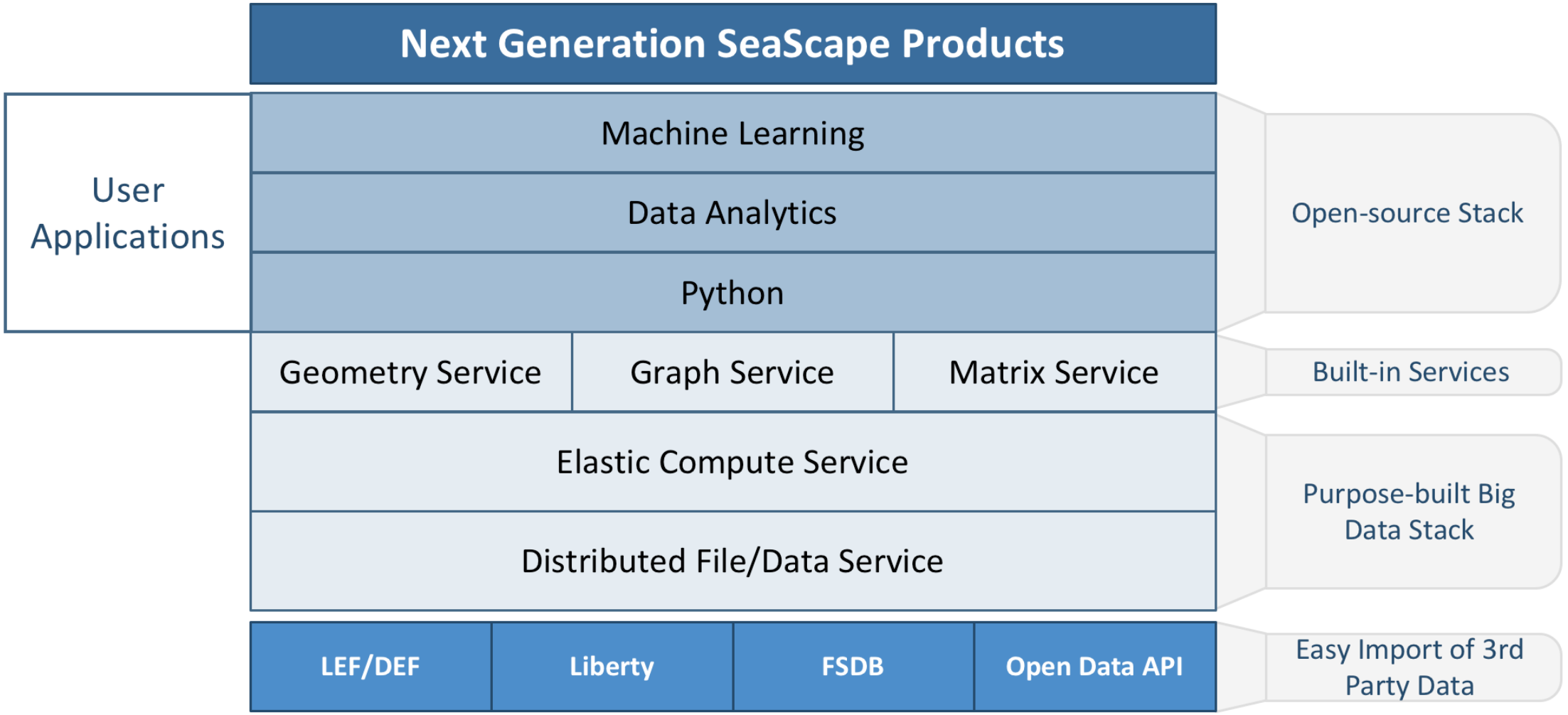
ANSYS SeaScape

Purpose-built big data platform for EDA To address multiphysics & multiscale challenges



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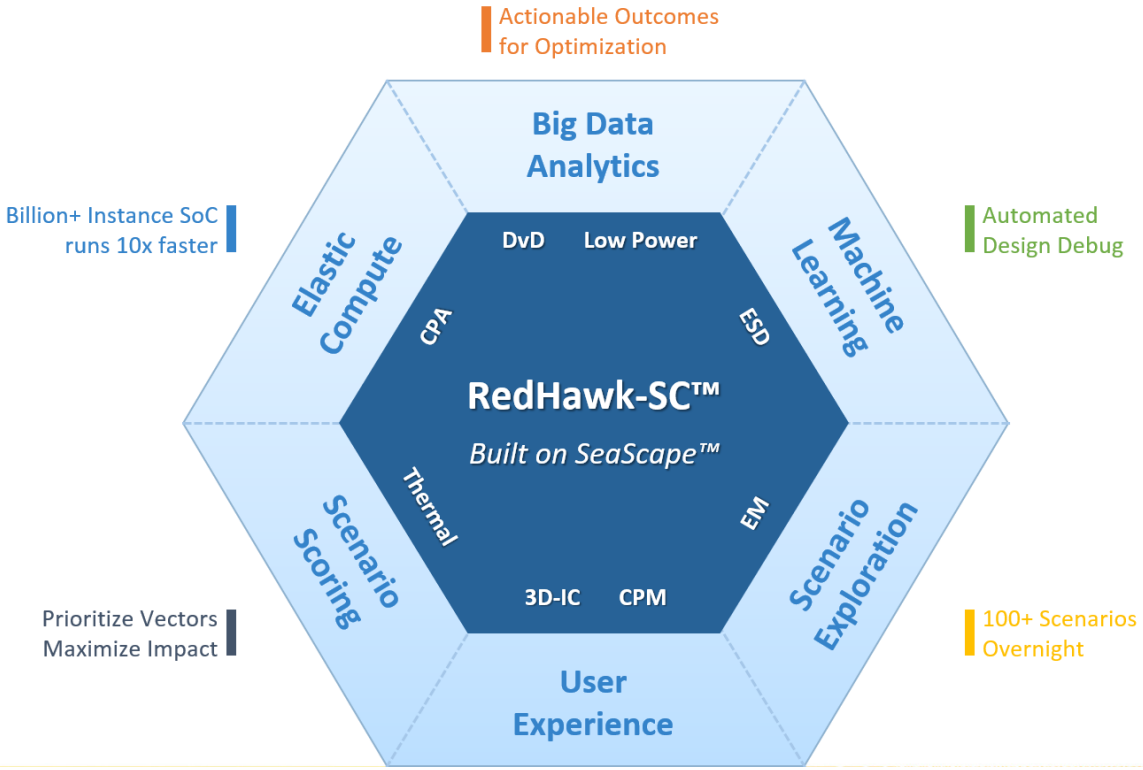
Accelerating Signoff for 7nm/5nm SoCs with RedHawk-SC

Benefits



Time to launch	**Instant**
Dedicated machines	**None**
Compute farm readiness	**Uses unused cores** Across busy queues, multiple queues and low memory queues
Turn Around Time (TAT) improvement (Elastic Compute vs. Distributed Compute)	**3x-10x** Benefit increases with increased node count, and/or CPU-cores
Core utilization improvement (Elastic Compute vs. Distributed Compute)	**5x-10x**

Accuracy **Capacity** **Coverage**

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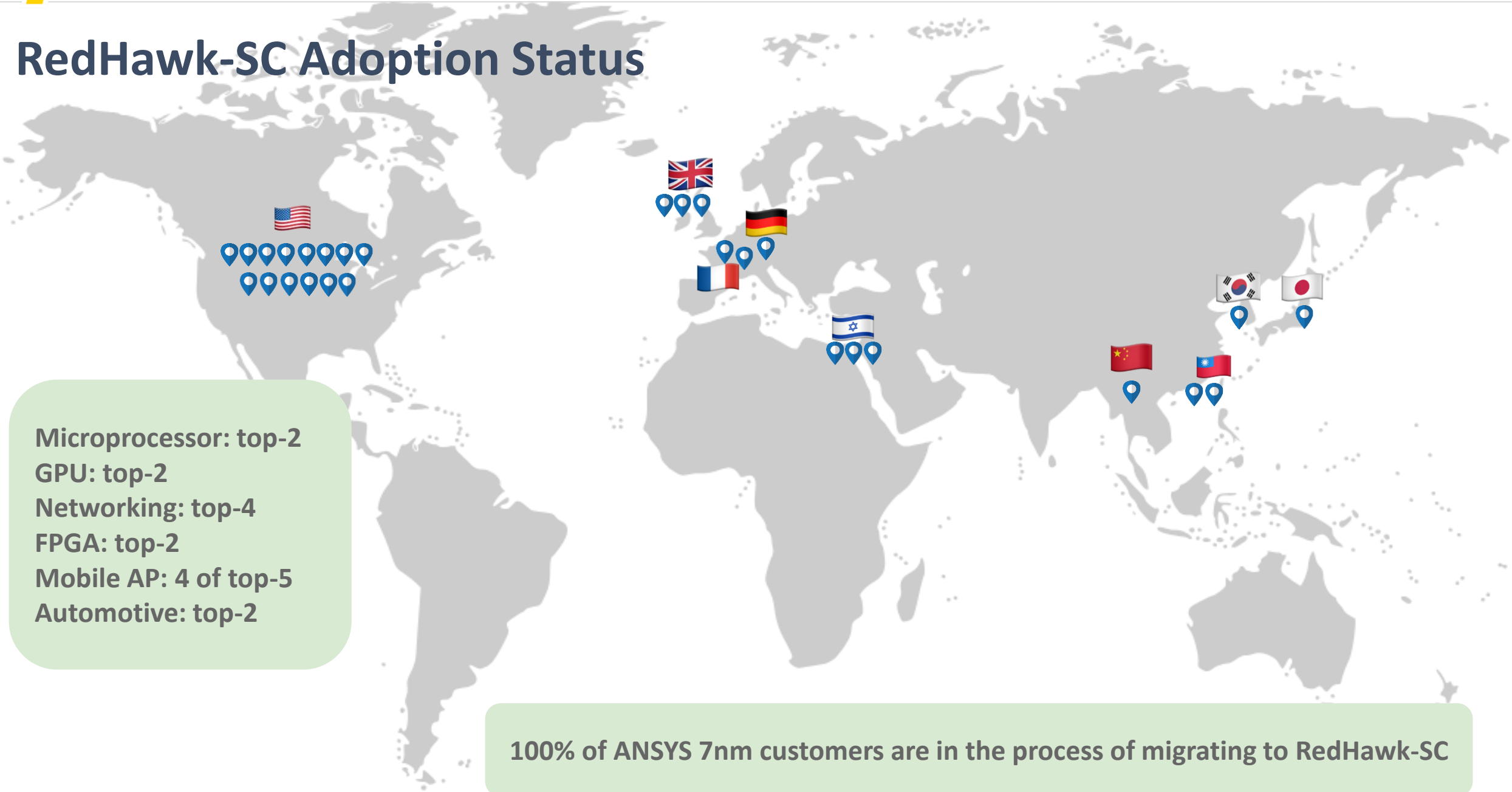
RedHawk-SC Adoption Status



Microprocessor: top-2
GPU: top-2
Networking: top-4
FPGA: top-2
Mobile AP: 4 of top-5
Automotive: top-2

100% of ANSYS 7nm customers are in the process of migrating to RedHawk-SC

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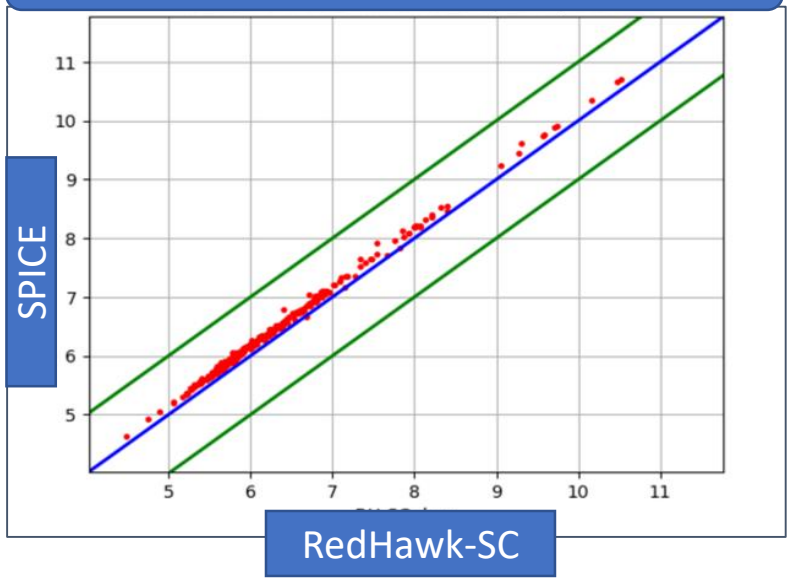
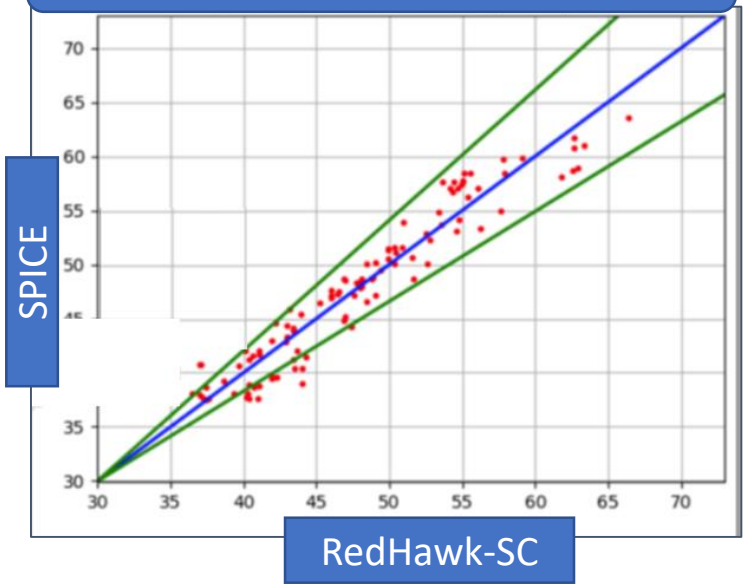
SPICE vs RedHawk-SC Correlation for Advanced FinFET Process Node

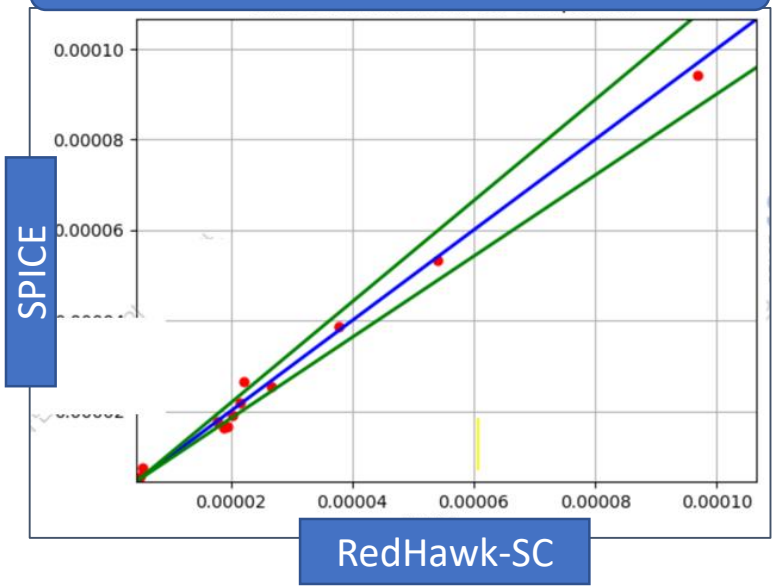
Static IR (mV)



Dynamic IR (mV)



Signal EM (A)



RedHawk-SC correlates very well with SPICE on Static IR, Dynamic IR and Signal EM

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RedHawk Fusion

Shift Left with Power Integrity

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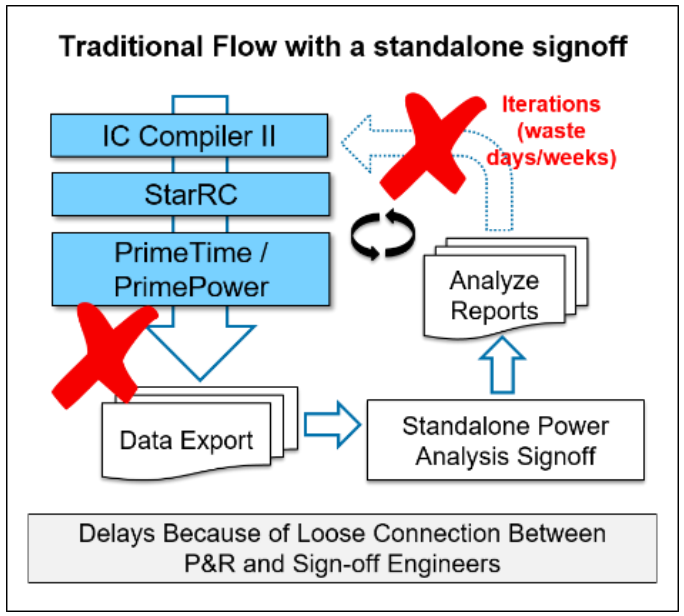
RedHawk Fusion - Shift Left with Power Integrity

Empowering Physical Design teams with Better Productivity and PPA



RedHawk Fusion - In-design Block-level IR-drop Optimization

IC Compiler II Fusion Compiler

RedHawk Fusion

RedHawk Signoff

ALL signoff scenarios (block/sub-system/full-chip)

- **Significant Improvement in Max IR Drop and # Violations**
- **Accelerated Block–level Closure Saving Days/Weeks**
- **Better Design PPA driven by Shift-Left in IR Drop Profile**

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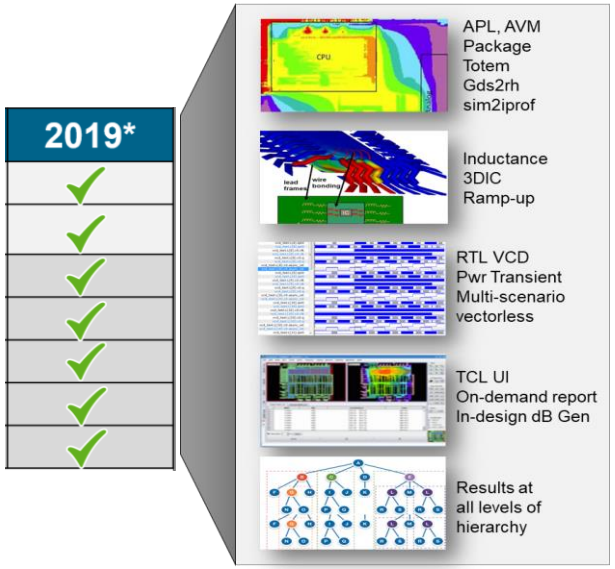
RedHawk Fusion - In-design Block-level IR-drop Optimization

Industry-leading Accuracy, Optimization and Advanced Node Support

Accuracy

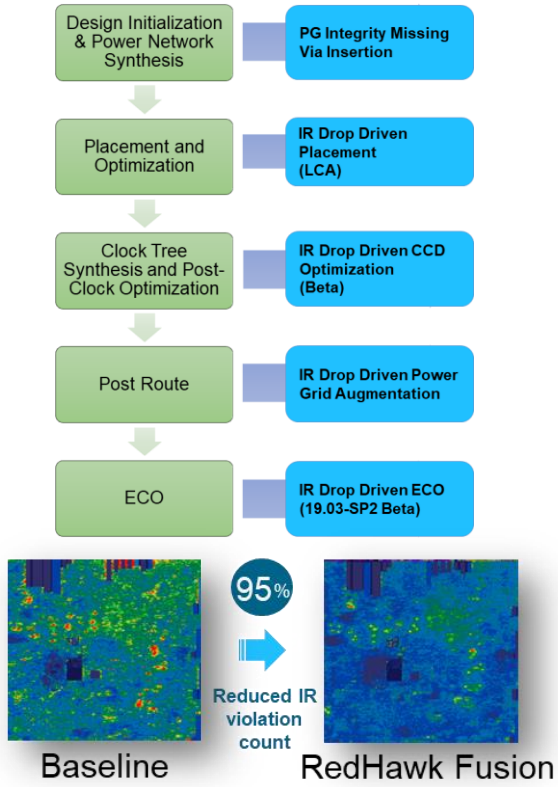
Block-level Signoff Accuracy



Power Grid, Power EM, Thermal
Static/Dynamic Controls, Gate-level VCD
Model and Macro Modeling Support
Advanced Technology Support
Advanced Dynamic Controls, RTL-level VCD
User Direct Access Results, Reports
Visibility at all Hierarchical Levels

Optimization

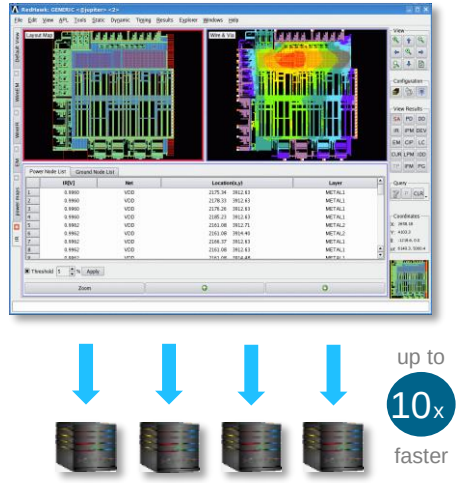
Robust Optimization in P&R



Advanced Nodes

RedHawk-SC Support

Next-generation RedHawk built on ANSYS SeaScape



Elastic compute scalability

Greater throughput / capacity

Same push-button flow

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RedHawk Fusion – Block-level Power Integrity Closure

1 Block Level Closure
For PD Engineers

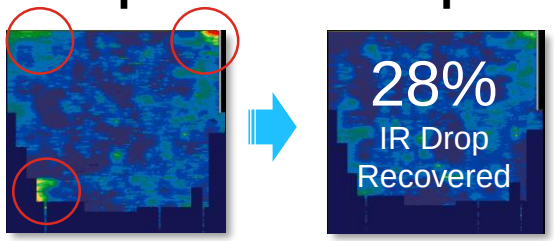
IC Compiler II
Fusion Compiler
RedHawk Fusion

RedHawk Signoff

ALL signoff scenarios
(block/sub-system/full-chip)

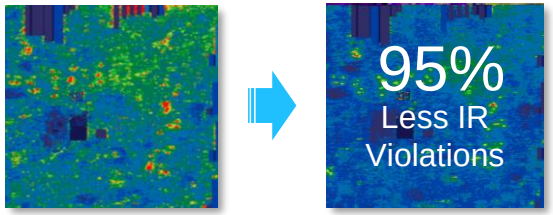
2 QoR Benefits
Improved IR Drop

Optimize IR Drop



Baseline Place+CTS+PGA

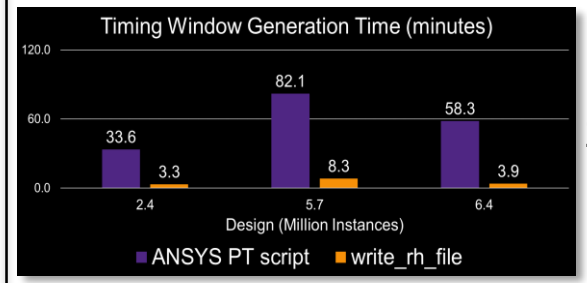
Reduce IR Violation Count



Baseline Place+PGA

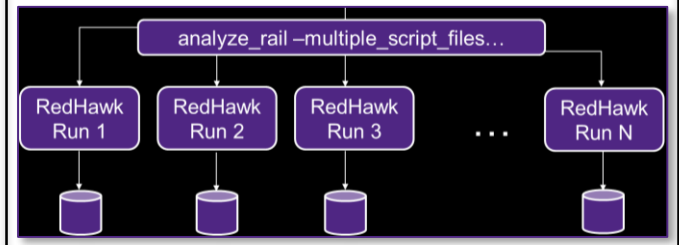
3 Productivity Benefits
Improved TTR

Auto-TWF/IPF Generation



up to 15x faster

Parallel Runs from ICCII



Note: All results are written to files outside of NDM.

Reduced ECO Iterations

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ICCII / Fusion Compiler Flow With RedHawk Fusion

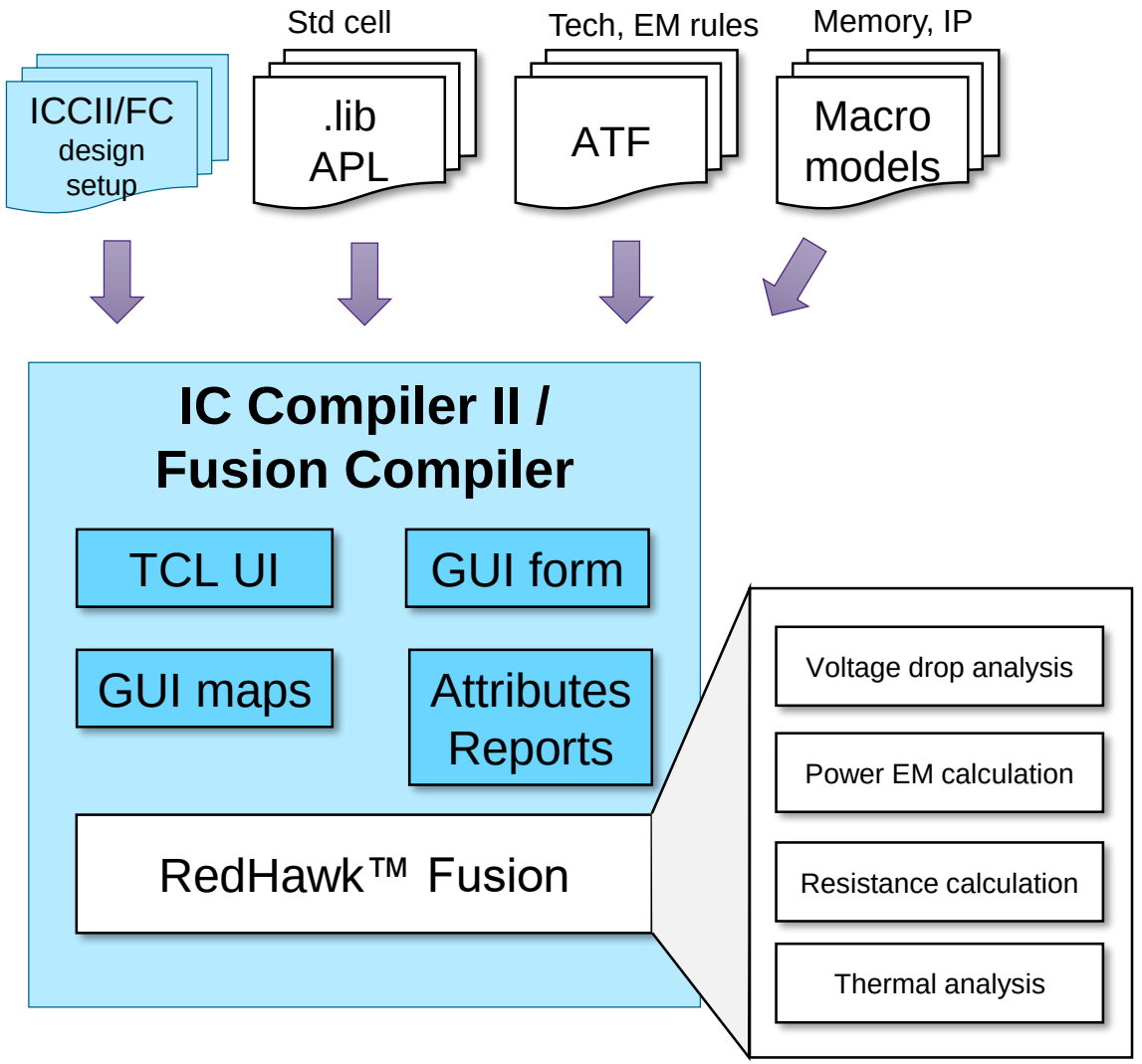
Input Data Requirements

- ICCII/FC Design Environment
  - NDM design with power routing
  - Setup including reference libraries, SDC constraints, activities for power analysis

- RedHawk Fusion Environment
  - Liberty files (.libs)
  - Cell models (APL files)
  - IP Models

    Technology files (ATF)
  - *GSR file (any custom settings will be included as a script in ICCII/FC)*
  - Required analysis and any custom settings

personalize settings



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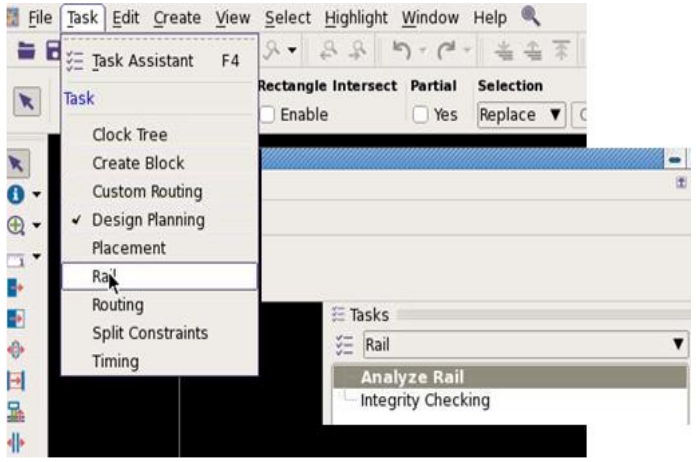
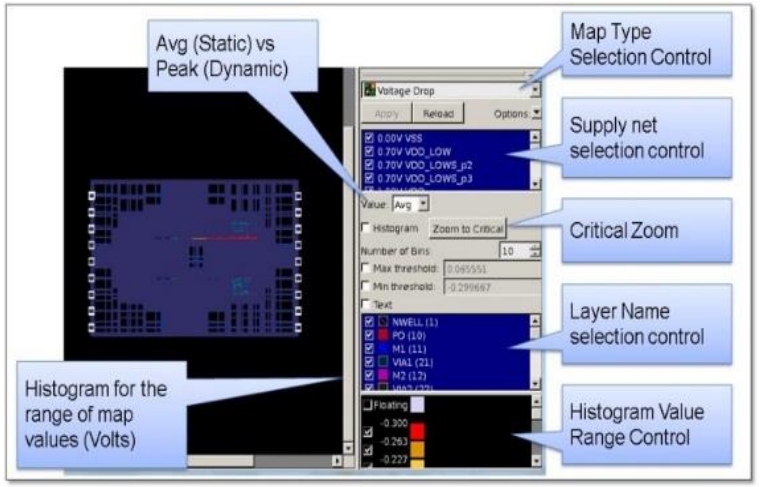
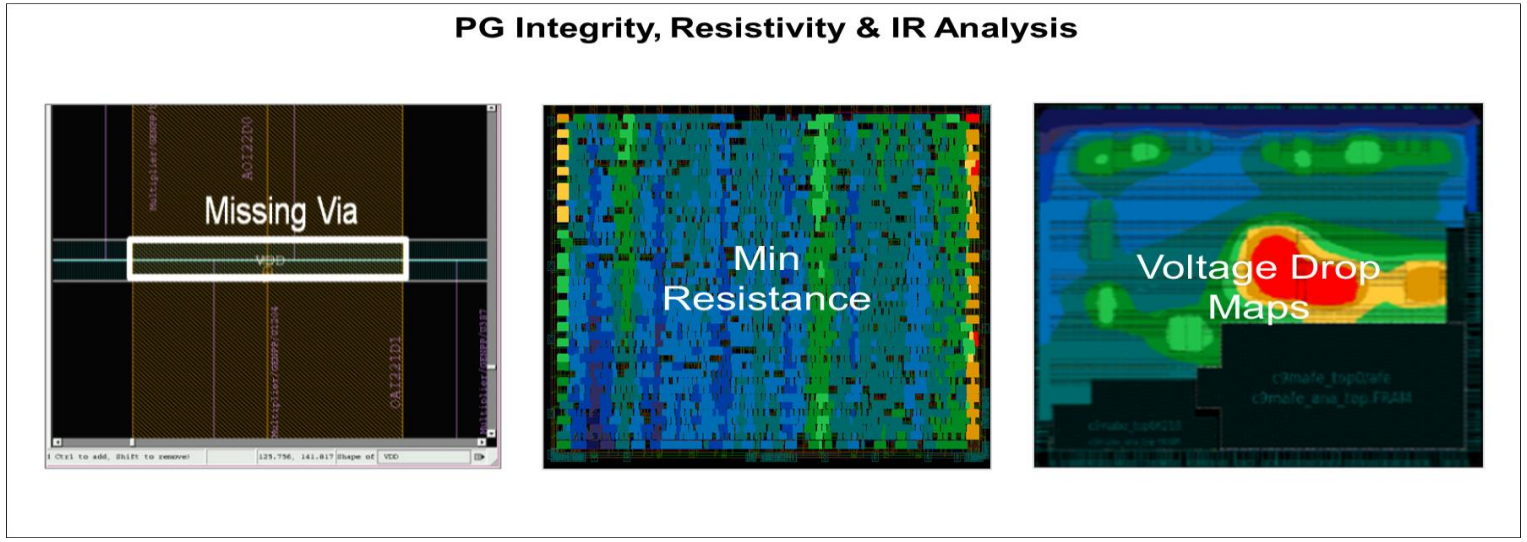
RedHawk Fusion within ICCII/Fusion Compiler Cockpit

One-Click Access





Comprehensive Maps



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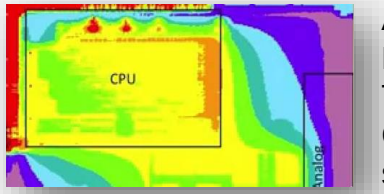
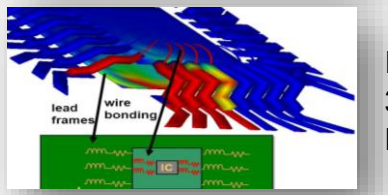
RedHawk Fusion Now with Block-level Signoff Accuracy

Key Block-level Signoff Features

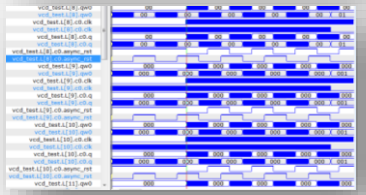
	2018	2019*
Power Grid, Power EM, Thermal	✓	✓
Static/Dynamic Controls, Gate-level VCD	✓	✓
Model and Macro Modeling Support	✓	✓
Advanced Technology Support	✓	✓
Advanced Dynamic Controls, RTL-level VCD		✓
User Direct Access Results, Reports		✓
Visibility at all Hierarchical Levels		✓



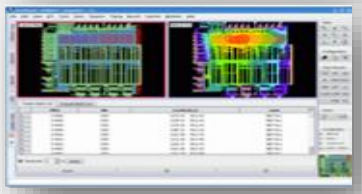
APL, AVM
Package
Totem
Gds2rh
sim2iprof



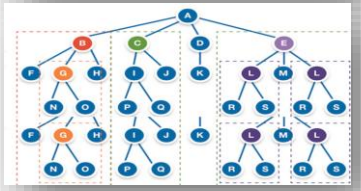
Inductance
3DIC
Ramp-up



RTL VCD
Pwr Transient
Multi-scenario
vectorless



TCL UI
On-demand report
In-design dB Gen



Results at
all levels of
hierarchy

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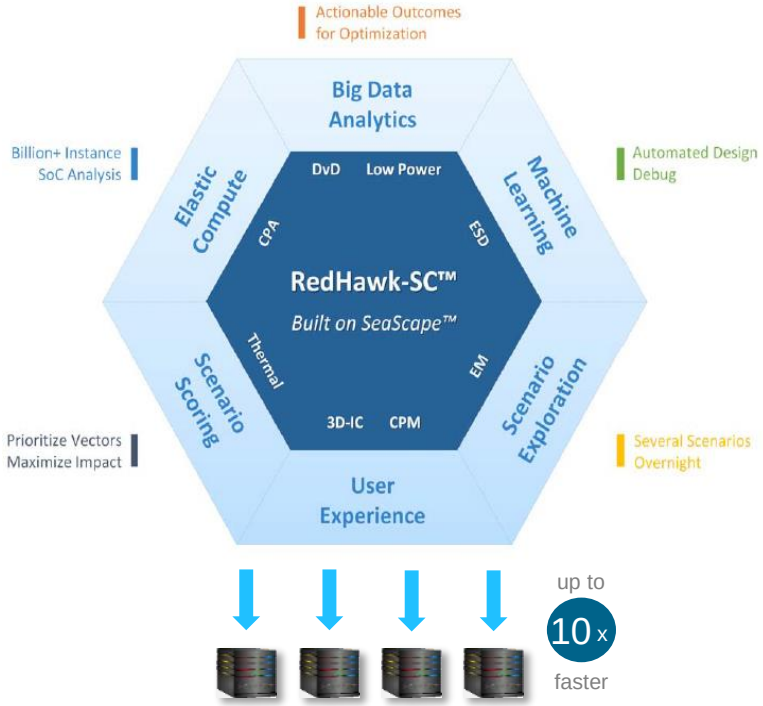
RedHawk-SC Fusion

Release 2019.03 includes RedHawk-SC integration

ANSYS RedHawk-SC

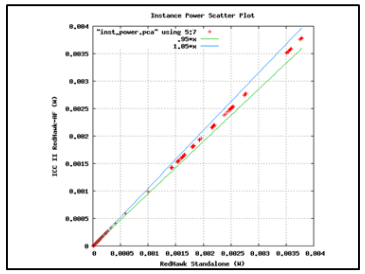


Next gen ANSYS platform
Sub 16nm design analysis
Greater throughput/capacity

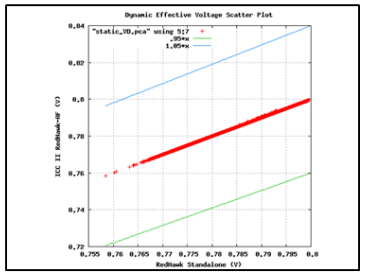
RedHawk-SC Fusion Accuracy
vs Standalone

100% Correlation (Arm Cortex-A75)

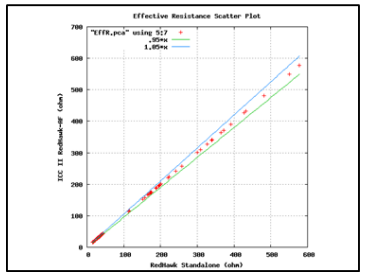
Instance Power



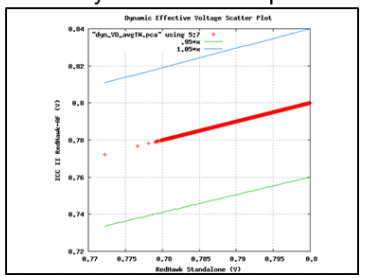
Static IR-Drop



PG Network Power



Dynamic IR-Drop



RedHawk-SC Fusion Flow
vs RedHawk

No difference in the flows

Just point to correct binary: RedHawk or RedHawk-SC

Same commands and app options across the flows

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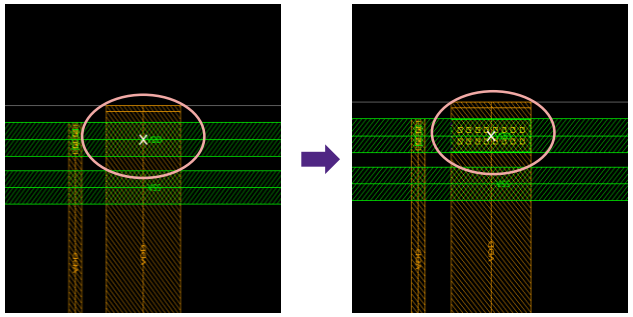
IR-Driven Optimization - Overview

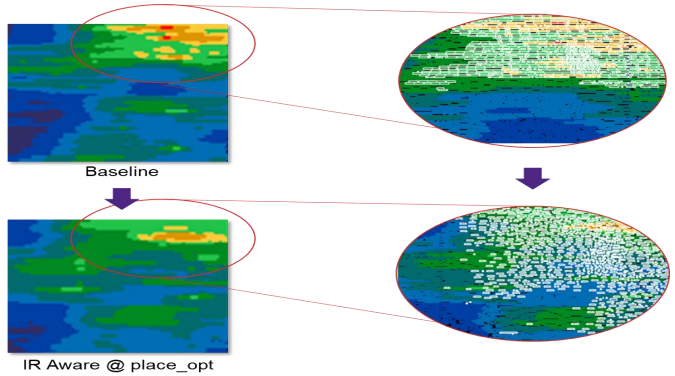
Rich feature set throughout the implementation flow

IR-Driven Via Insertion



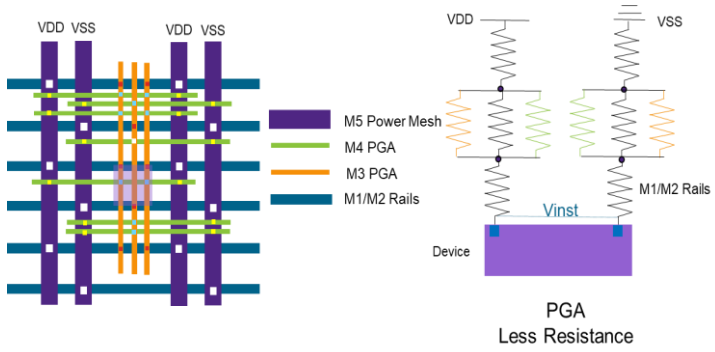
Extraction and analysis based – DRC aware

IR-Driven Placement



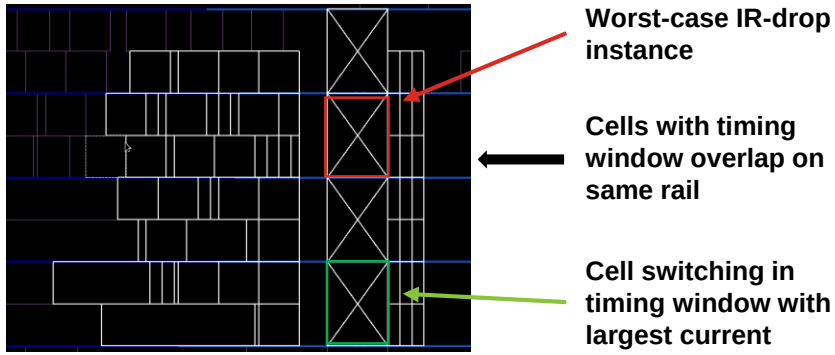
Cell spreading at placement and CTS – Timing/conges aware

IR-Driven PG Augmentation



Adding additional metal shapes – DRC/timing/EM aware

IR-Driven ECO



Down-sizing, load-splitting, relocation – timing aware

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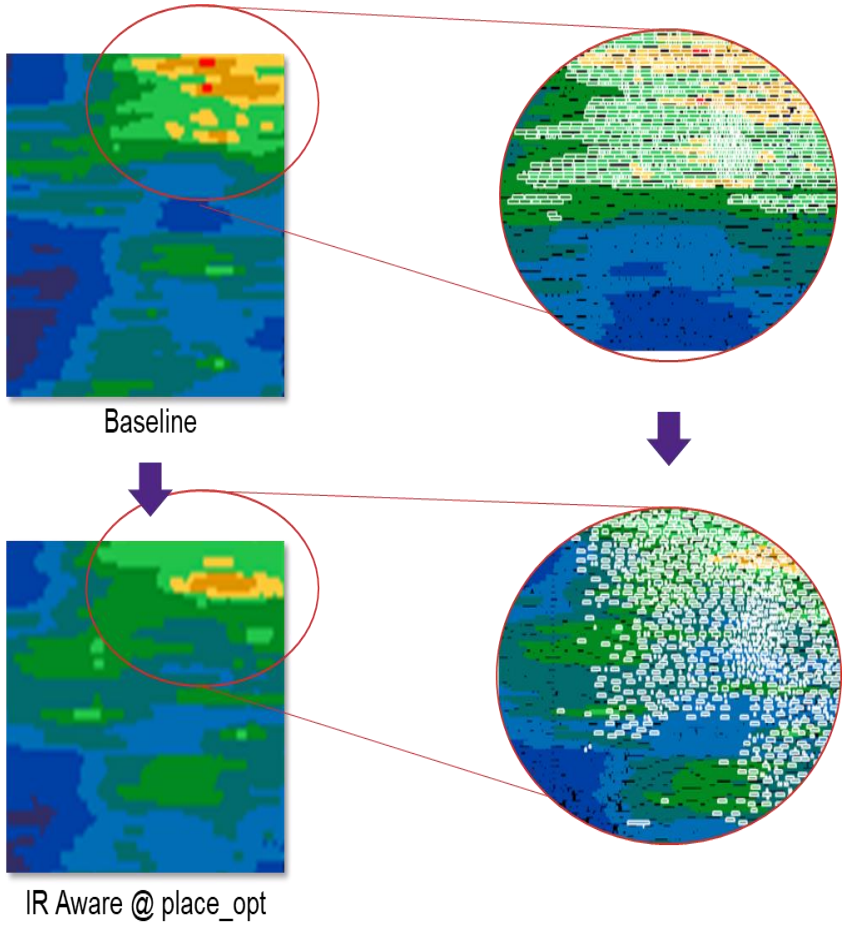
IR-Driven Placement

Methodology and Flow



Usage Flows in ICC-II/FC

- place_opt –to final_place
- Redhawk In-Design Vdrop Analysis
- place_opt –from final_place
- Redhawk In-Design Vdrop Analysis

- clock_opt –to route_clock
- Redhawk In-Design Vdrop Analysis
- clock_opt –from final_opto
- Redhawk In-Design Vdrop Analysis

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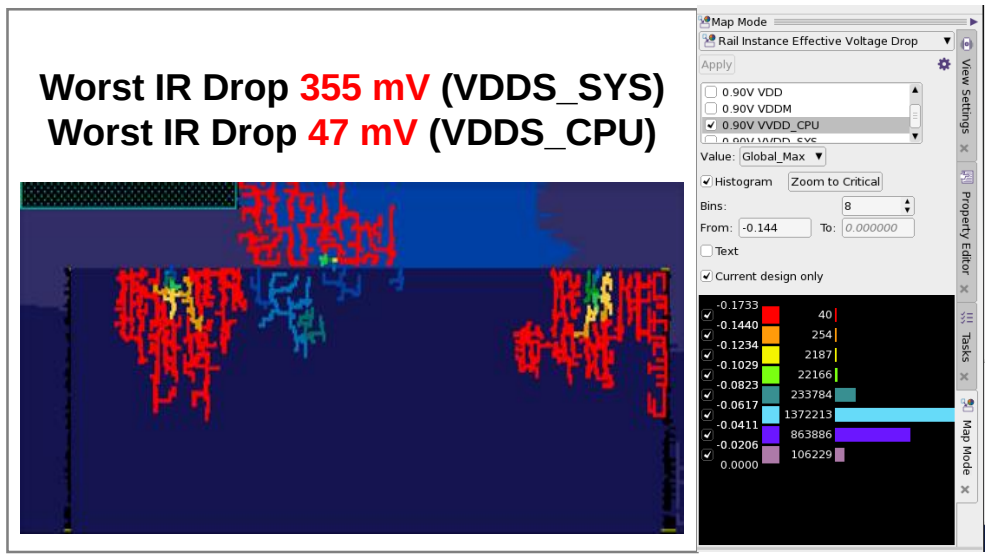
RedHawk Fusion – High-Performance Arm® Cortex®-A76

Available in the QiK flow

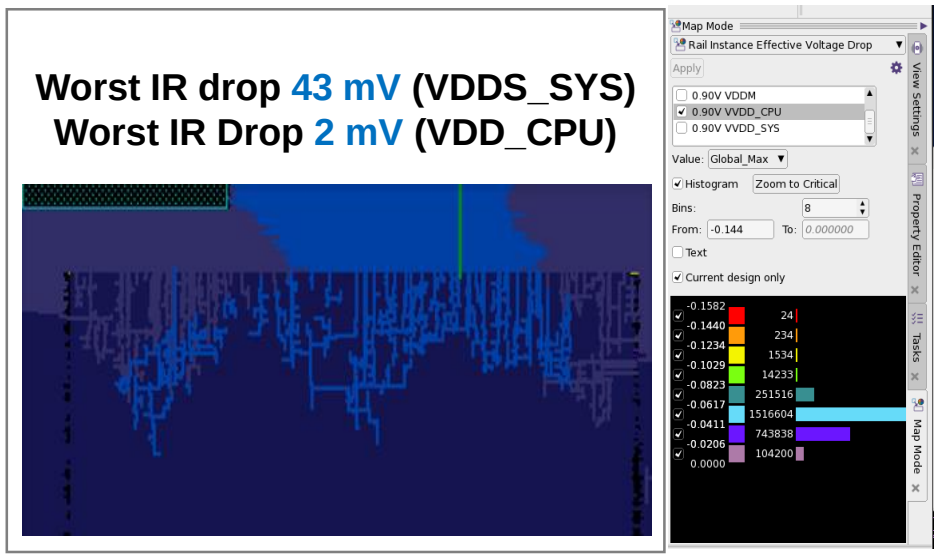
Baseline

Worst IR Drop 355 mV (VDDS_SYS)
Worst IR Drop 47 mV (VDDS_CPU)



IR Driven Placement

Worst IR drop 43 mV (VDDS_SYS)
Worst IR Drop 2 mV (VDD_CPU)



90%

Reduction in Peak IR drop value
(from 355mV to 43mV)
(from 47mV to 2mV)

35%

Reduction in # IR drop violations
(from 24647 to 16025)

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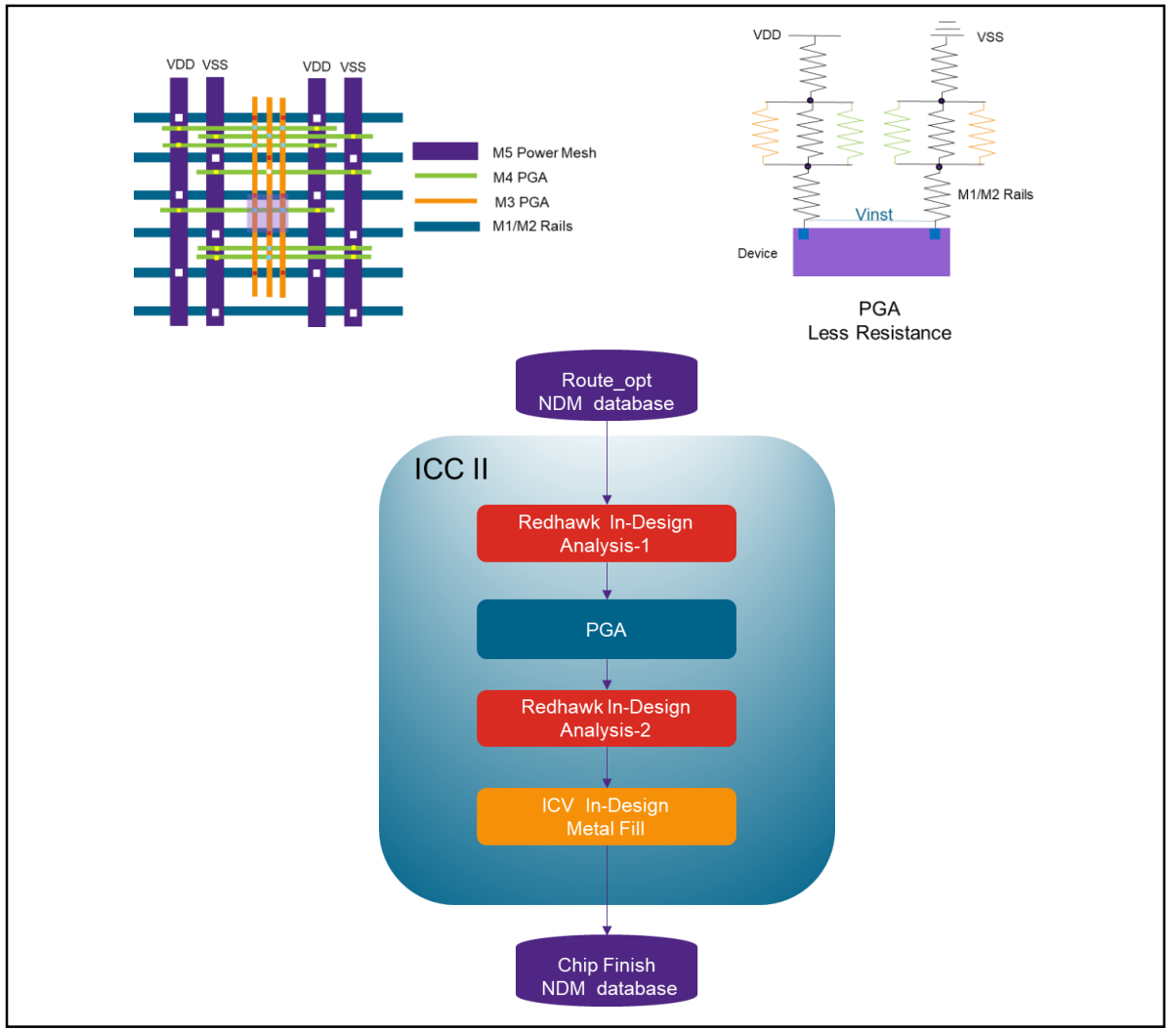
IR-Aware PG Augmentation

Methodology and Flow

- PGA segments acts as parallel resistors
  - reducing the resistance of the power grid and improving the instance voltage drop.
- Augmentation is designed to be DRC Neutral
  - Tech file driven, will honor all necessary tech-file rules.
- Augmentation is IR Drop Aware
  - Targeted fixing can focus Augmentation where required and minimize possible negative timing impact.
- Timing aware.
  - User can manually specify critical nets and slack threshold to control impact on timing
- Multi PG support, for multi voltage designs.
  - PGA runs on a PG Pair, multi PG designs will need multiple PGA runs.
- Include/Exclude regions for PGA
  - PGA can be targeted to or excluded from particular areas.



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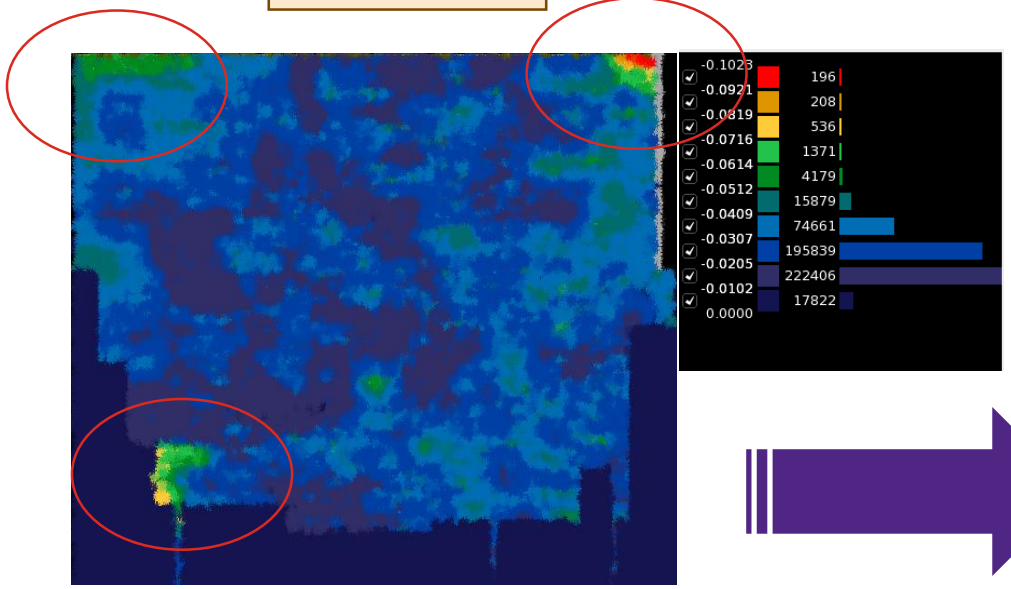
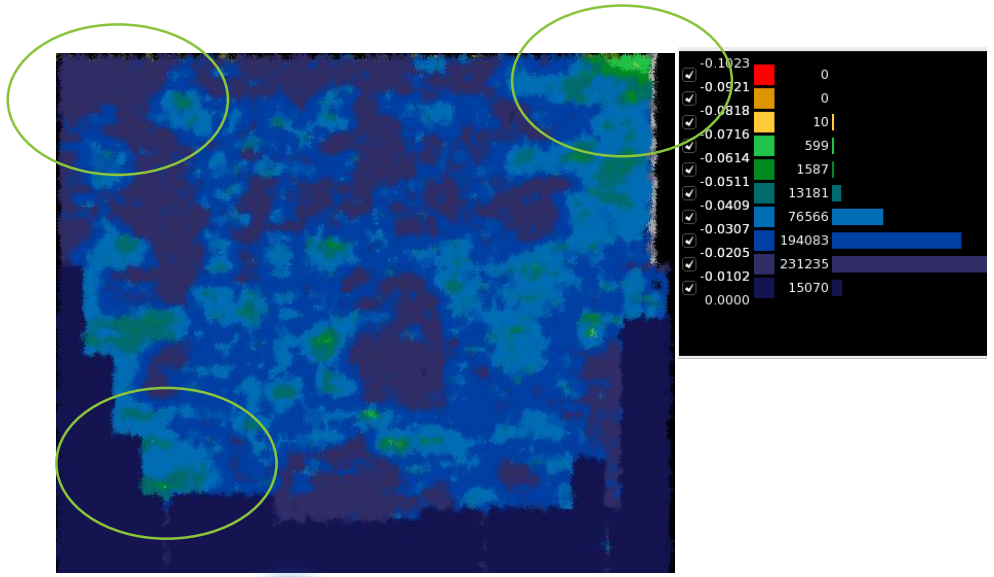
RedHawk Fusion – High-Performance Arm® Cortex®-A53

Deployed in FinFET Production Flow

Baseline



IR Driven Opt (Place + CTS + PGA)



Experiment	# DRCs	WNS, ns	TNS, ns	Max IR Drop, mV
Baseline	855	-0.310	-1077	**102**
IR-Drop Driven Opt	265	-0.264	-675	**73**

99% **Reduction in # IR drop violations**
(from 940 to 10)

28% **Reduction in Peak IR drop value**
(from 102mV to 73mV)

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RedHawk Analysis Fusion Roadmap

Analysis

- Root Cause IR Analysis
  - *Release 2019.03*
- Thermal Analysis for RedHawk-SC
  - *Release 2019.03-SP4*
- 3DIC Support
  - *Release 2019.12*
- ML Incremental IR Analysis
  - *Release 2019.12*
- Power Switch Cell Analysis
  - *Release 2020.09*

Performance and Capacity

- Hierarchical Support: Automated Block Context Generation
  - *Release 2019.03-SP2*
- Non-blocking ICC II Prompt
  - *Release 2019.03-SP2*
- Power Switch Cell Optimization
  - *Release 2020.09*
- Power EM Fixing
  - *Release 2020.09*
- ML IR-driven PG synthesis
  - *Release 2020.09*

Optimization

- IR Drop-Driven ECO Fusion
  - *Release 2019.03-SP4*
- IR Drop-Driven CCD (Beta)
  - *Release 2019.03-SP2*
- Multi-Scenario Based IR Drop-Driven Optimization
  - *Release 2019.12*
- Multi-parameter-driven fixing for RedHawk-SC
  - *Release 2020.09*

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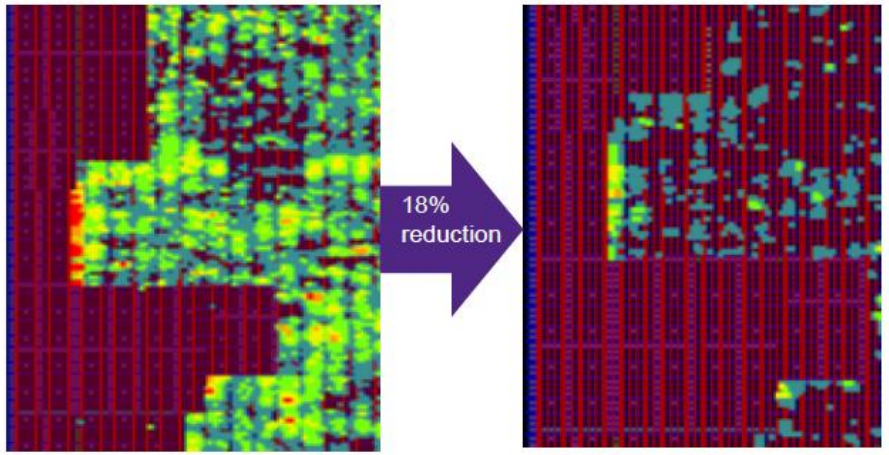
RedHawk Fusion – Automotive SoC Tapeout (8/7nm)

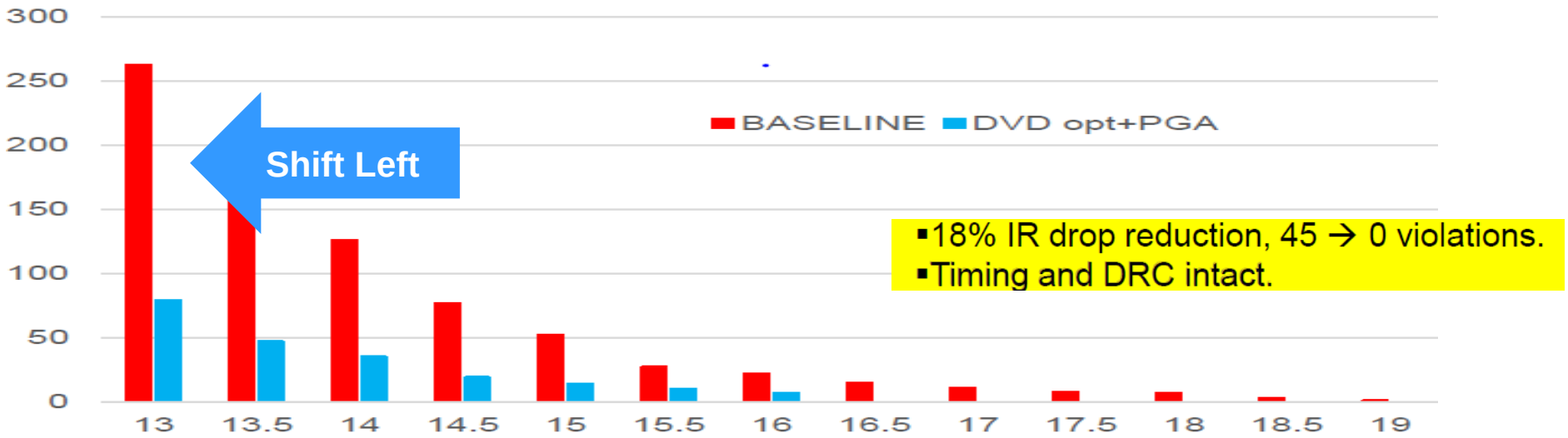
Arm Cortex-A76



Baseline

DvD aware Place+PGA

8 → ~2 eco iterations



In-design RedHawk Fusion Accelerates Block-level Power Integrity Closure

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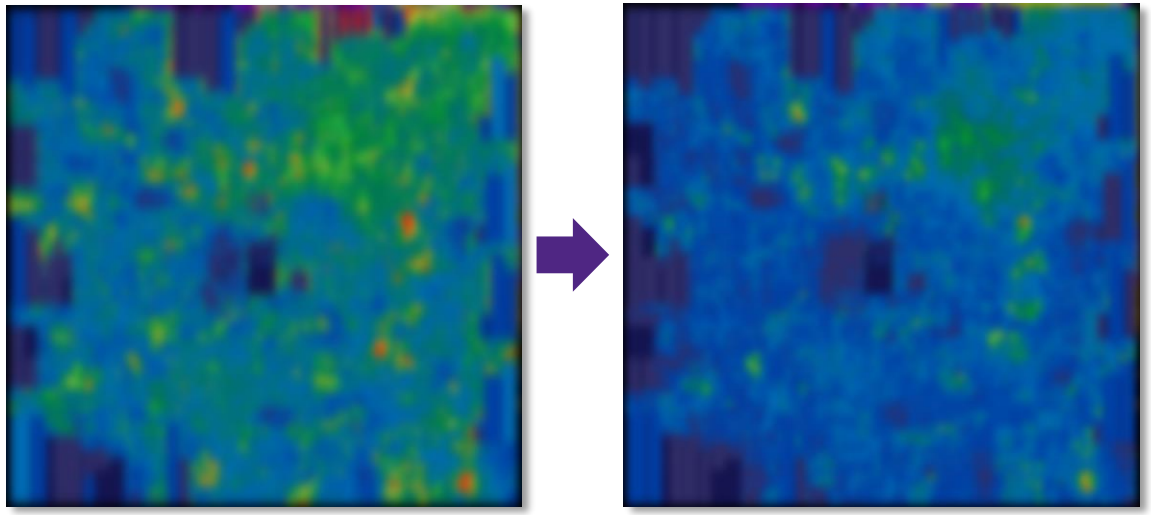
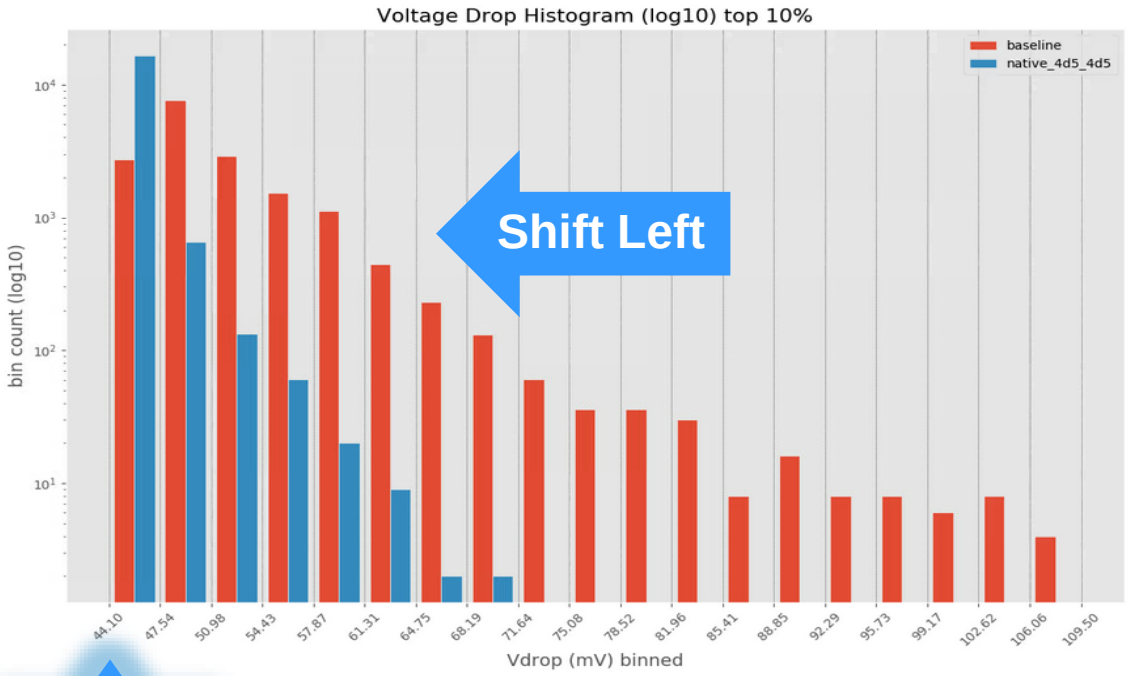
RedHawk Fusion – Leading-edge GPU Customer



Baseline IR Aware Flow

Baseline		IR Aware Flow	
IR drop violations # cells (% cells)		**IR drop violations** # cells (% cells)	
>= 4.5%	**>= 8.0%**	>= 4.5%	**>= 8.0%**
98,386 (7.557%)	**3,136** (0.241%)	18904 (1.452%)	**147** (0.011%)



95% **Reduction in # IR drop violations** (from 3136 to 147)

36% **Reduction in Peak IR drop value** (from 106.1mV to 68.2mV)

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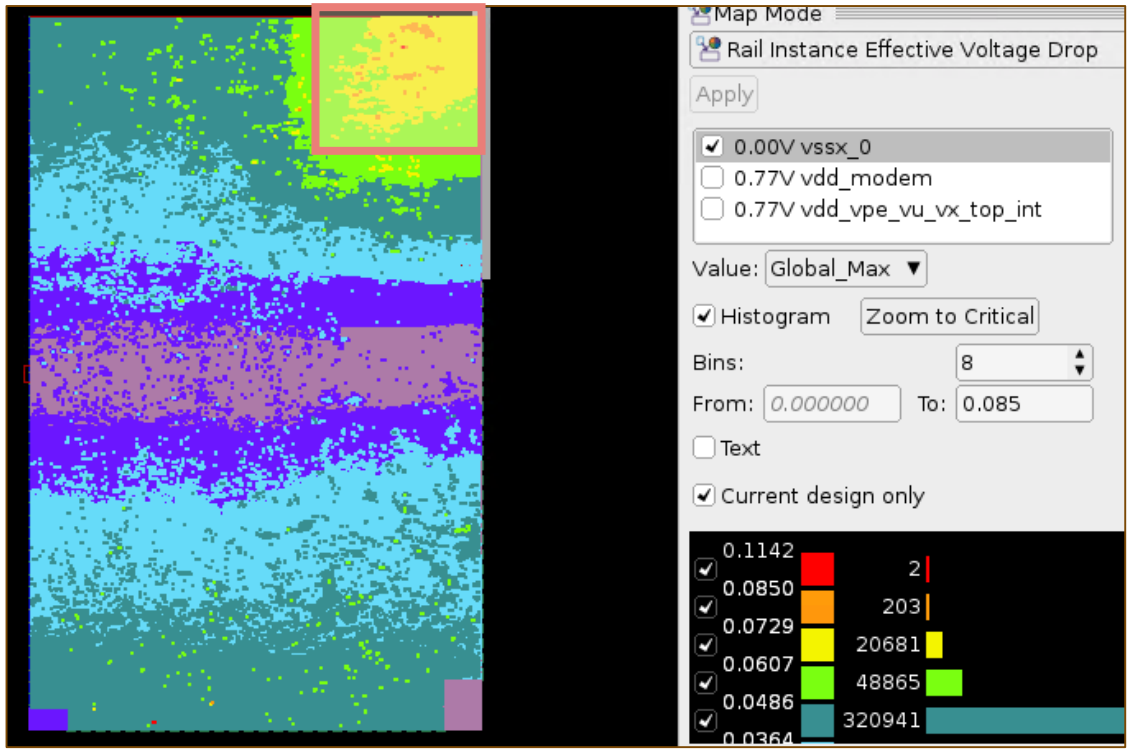
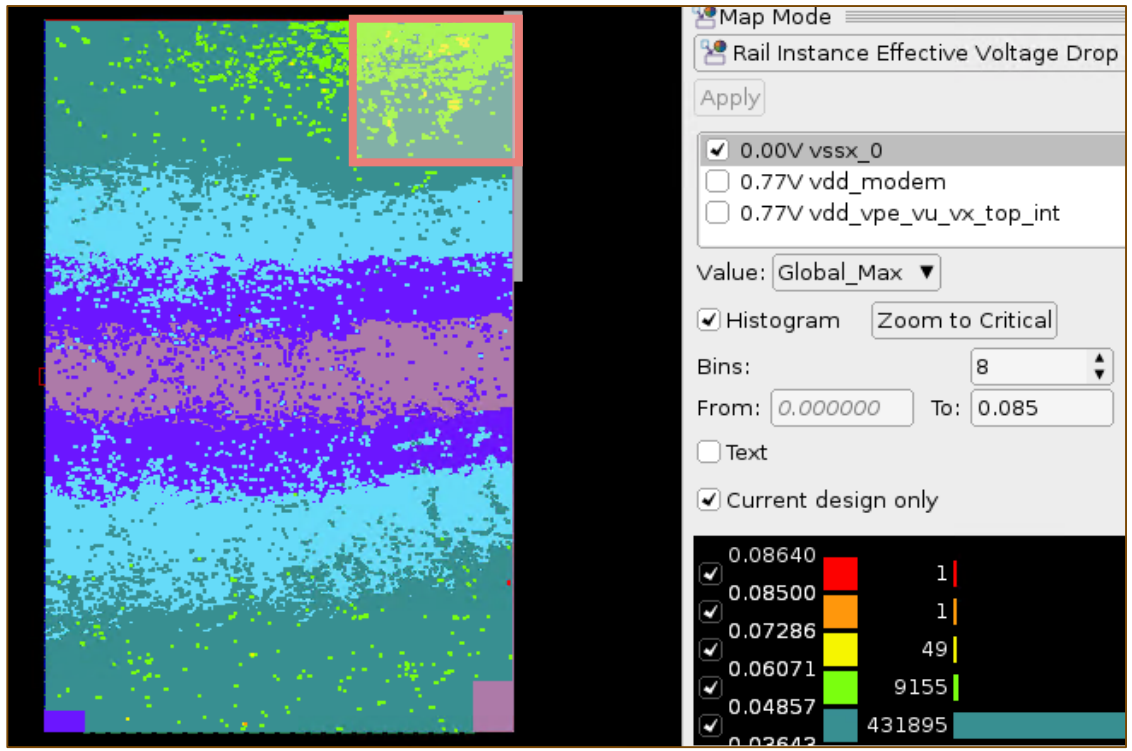
RedHawk Fusion – Mobile/Communications Design Leader

Baseline



IR Driven Placement



99% **Reduction in # IR drop violations**

24% **Reduction in Peak IR drop value**

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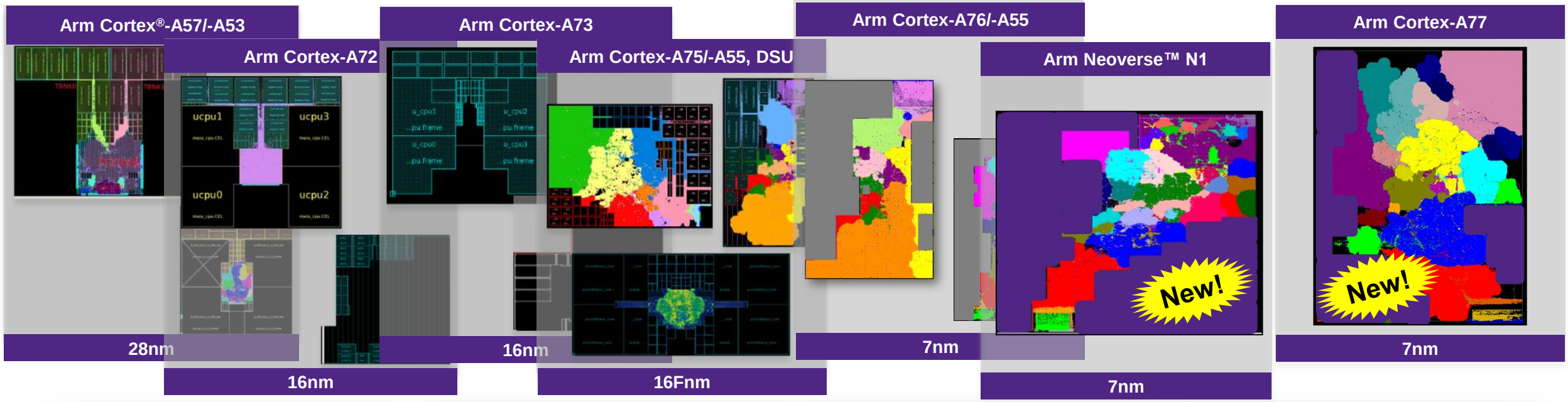
Synopsys QIKs for Advanced Arm® Cores

Reference Flows and Guides to Meet PPA Targets using Arm Artisan® IP



QIKs available to Arm-Synopsys customers, go to www.synopsys.com/Arm

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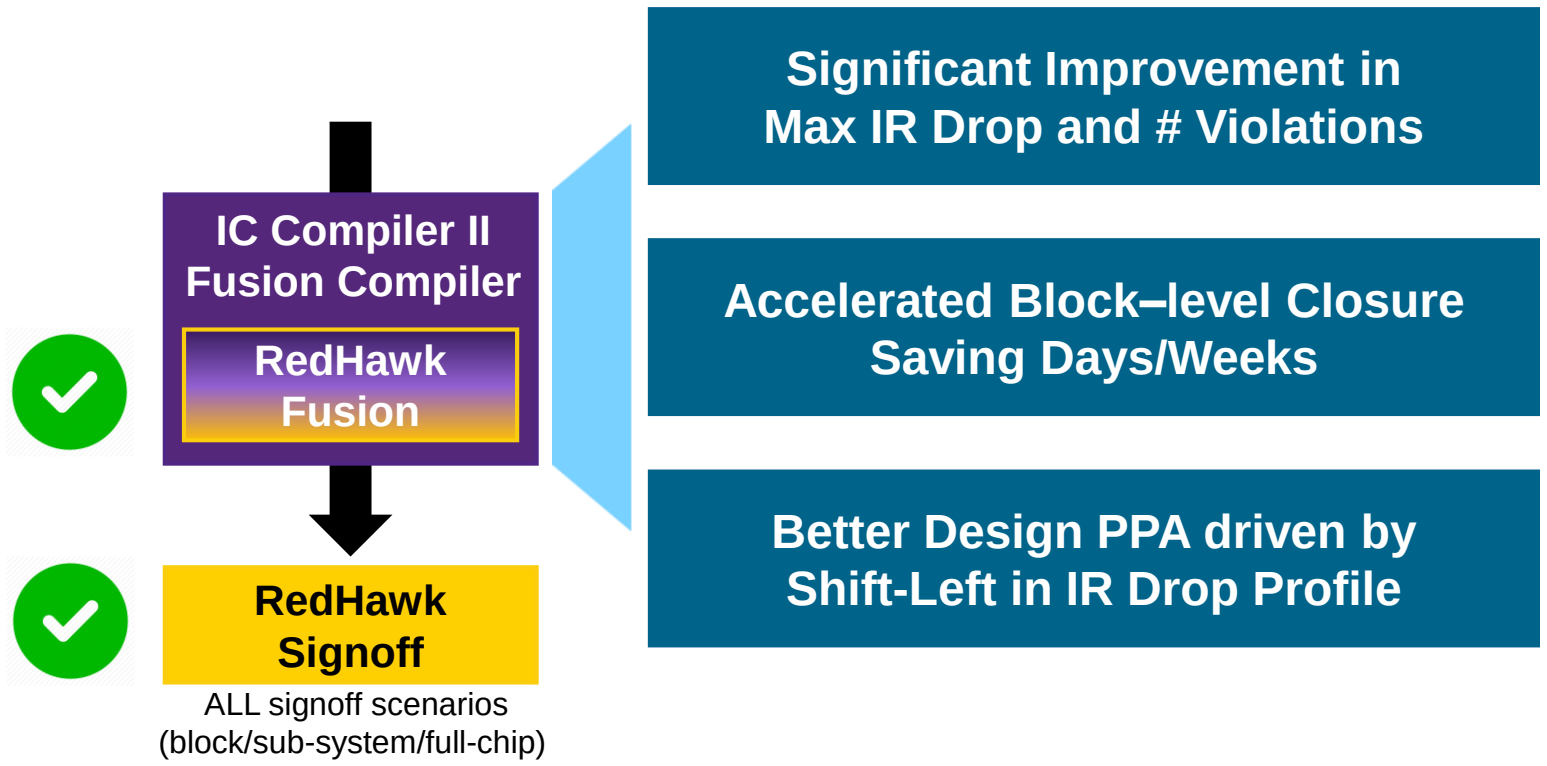
RedHawk Fusion - Summary

Accelerate Power and Rail Integrity Closure on the Latest Armv8-A Processors

RedHawk Fusion - In-design Block-level IR-drop Optimization

Empowering Physical Design teams with Better Productivity and PPA



Significant Customer Deployment, Multiple Tape-outs at Advanced 8/7nm Process Nodes

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