

ARM at Cray

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arm

ARM at Cray



Collaborations

- DOE Cray Fast Forward 2 and PathForward programs
- Contributed to SVE and other aspects of ARM ISA

Systems

- Cray XC50 "Scout"

Software

- Full Cray programming environment support
- Same management system and operating environment (Linux) as for x86

Cray Collaboration Evident in ARM SVE



Feature	Benefit
Scalable vector length (VL)	Increased parallelism while allowing implementation choice of VL
VL agnostic (VLA) programming	Supports a programming paradigm of write-once, run-anywhere scalable vector code
Gather-load & Scatter-store	Enables vectorization of complex data structures with non-linear access patterns
Per-lane predication	Enables vectorization of complex, nested control code containing side effects and avoidance of loop heads and tails (particularly for VLA)
Predicate-driven loop control and management	Reduces vectorization overhead relative to scalar code
Vector partitioning and SW managed speculation	Permits vectorization of uncounted loops with data-dependent exits
Extended integer and floating-point horizontal reductions	Allows vectorization of more types of reducible loop-carried dependencies
Scalarized intra-vector sub-loops	Supports vectorization of loops containing complex loop-carried dependencies

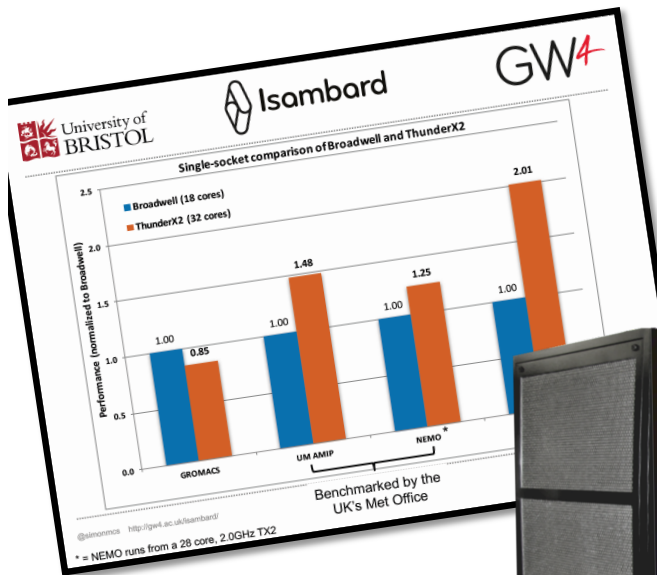
Nigel Stephens – <https://community.arm.com/processors/b/blog/posts/technology-update-the-scalable-vector-extension-sve-for-the-armv8-a-architecture>

ARM is in the Cray XC50

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CRAY XC50 – LEADING SUPPORT FOR ARM IN HPC



“Having access to Cray’s optimised HPC software stack of compilers and libraries in addition to all of the open source tools has been a real advantage.”

-- Prof. Simon McIntosh-Smith
University of Bristol and GW4

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ARM IS THE NNSA’S NEW SECRET WEAPON

November 7, 2018 Nicole Hemsoth



“Every time we get more memory bandwidth, we go faster. But when you give us FLOPS, we don’t. We just wait for memory more often and we are looking for a better way to do this for our codes.”

-- Gary Grider
Los Alamos National Lab

THE GW4 ARM HACKATHON WAS BORING*

Applications	 
Arm v8 Compilers	 
Profilers	 

* It was boring because all of these codes “just worked”

Thunder X2 Processor Daughter Card

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2-Socket Nodes

8 DIMMs per Socket

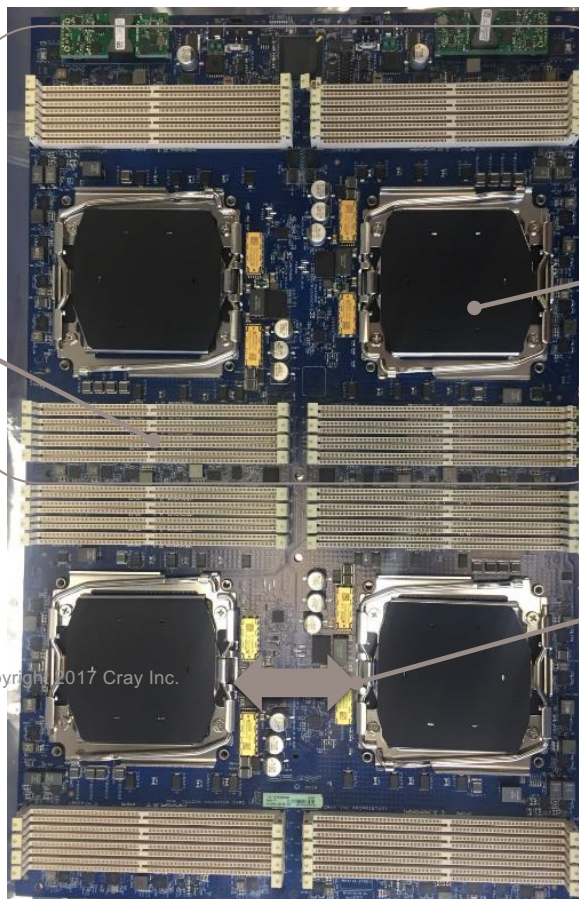
High memory and inter-chip link bandwidth permit a flat (uniform) 300 GB/s local memory system!

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ThunderX2 Processor
32 Cores
2.1 GHz base frequency + boost
537 Gflops
32 MB L3 Cache

Inter-chip Interconnect
75 GB/s/dir
24 lanes @
25 Gbps



Shasta Compute Infrastructures

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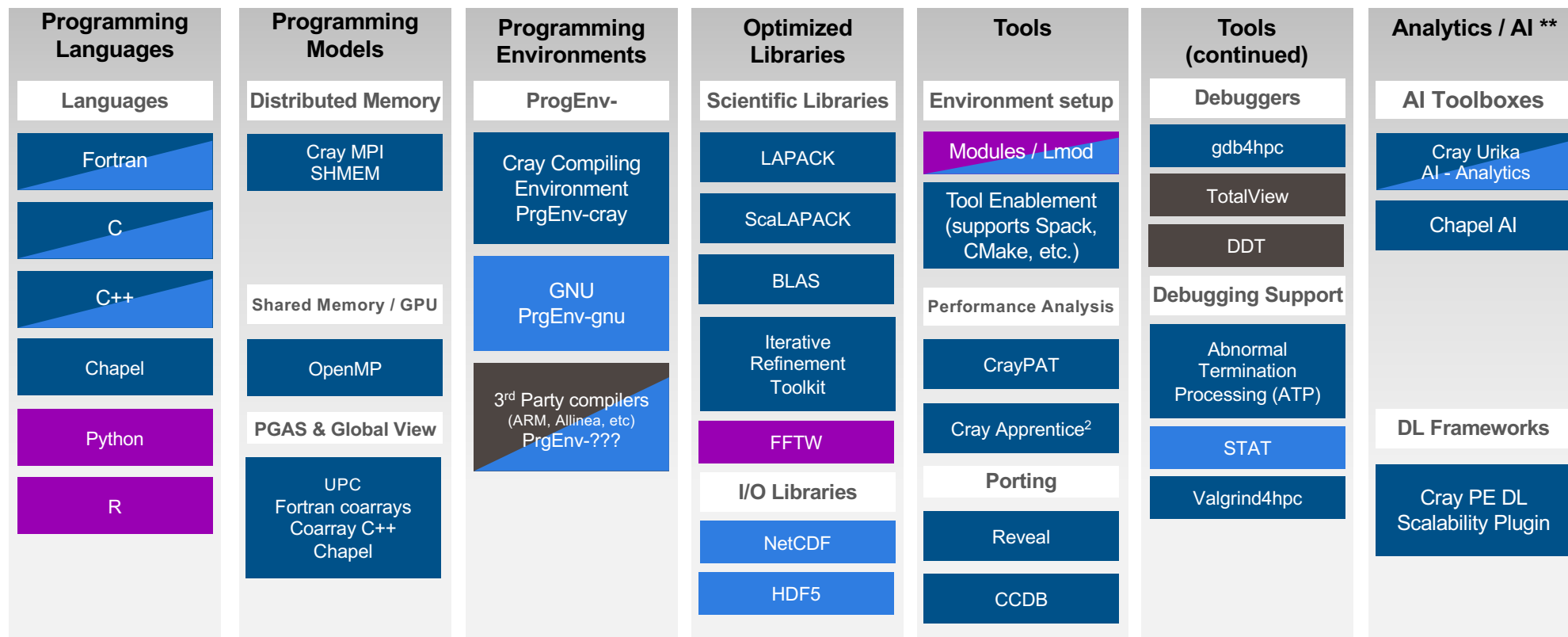
MOUNTAIN
Optimized Cabinet

RIVER
Standard 19" Rack



Same Interconnect – Same Software Environment

Shasta Development Environment



Cray Developed
 3rd party packaging
 Cray added value to 3rd party
 Licensed ISV SW

** Not PE dependent

SAFE HARBOR STATEMENT

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These statements are only predictions and actual results may materially vary from those projected. Please refer to Cray's documents filed with the SEC from time to time concerning factors that could affect the Company and these forward-looking statements.



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QUESTIONS?



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