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# Arm Enabling Research: SoC Labs workshop

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# Welcome and Introductions

# Agenda

- 11:00 – 12:30 : RE and Education keynotes
  - Executive introduction (10 min) – John Goodenough
  - Arm Flexible Access for Research and Arm Research SoC Labs (20 min) – Plout Galatsopoulos
  - DesignStart A5 launch (20 min) – Kobus Marneweck
  - Arm Education plans (20 min) – John Goodenough
  - Harvard SoC designs (20 min) – Paul Whatmough
- 12:30 – 14:00 : Lunch break
- 14:00 – 15:30 : Technical slots I
  - Arm Flexible Access for Research Technical offerings (30 min) – Liam Dillon
  - Debug and Trace, why bother? (30 min) – Liam Dillon
  - The OpenROAD project (30 min) – Andrew Kahng
- 15:30 – 16:00 : Coffee break
- 16:00 – 16:45 : Technical slots II
  - Arm Coherent Accelerator Interface (20 min) – Tutu Ajayi
  - Introduction to Europractice (15 min)– Mark Willoughby
- 16:45 – 17:30 : Open Q&A / Discussions

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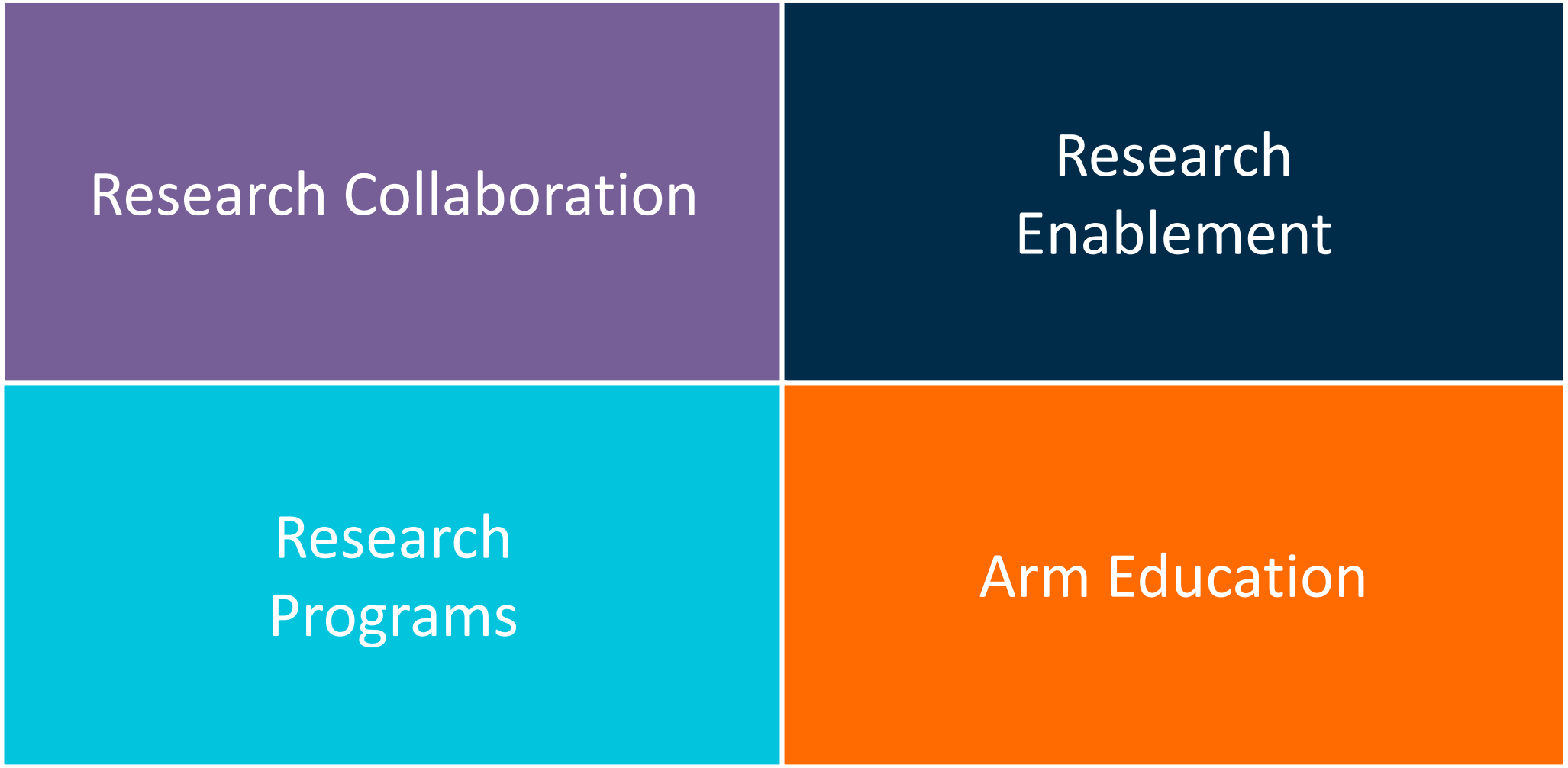
# Arm Research Enablement: Offerings and Impact

# Introducing Arm Research



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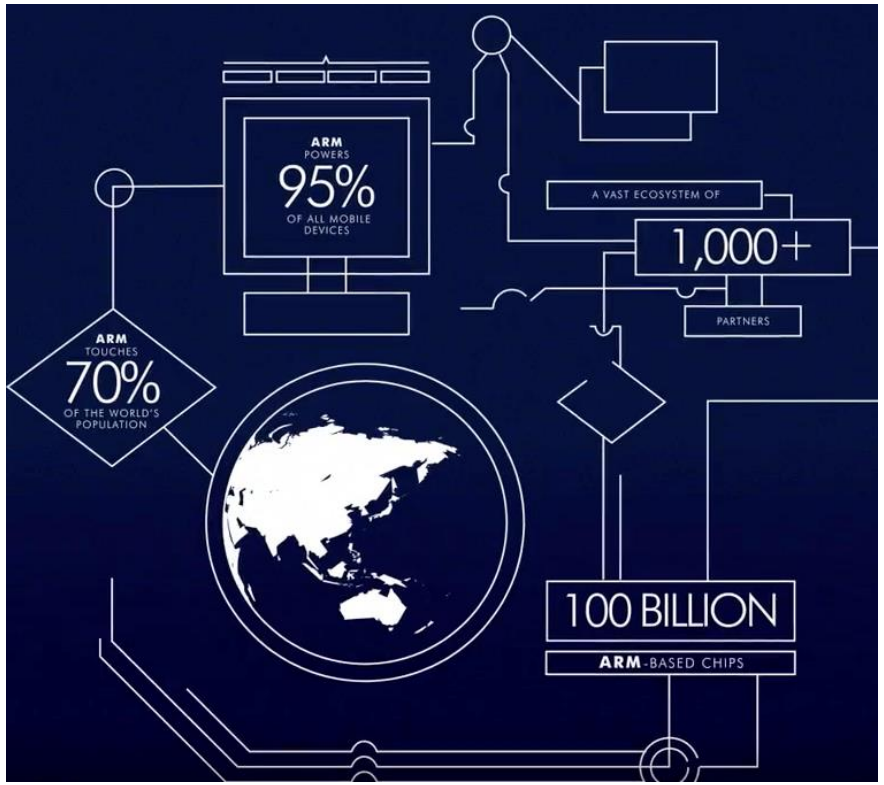
# Arm Research Collaboration and Enablement Program

**For more than 25 years, Arm has developed unique expertise, fueled the growth of semiconductor industry, built and nurtured vibrant ecosystems around a wide range technologies.**

## Bringing our products, partnerships and expertise to the research community



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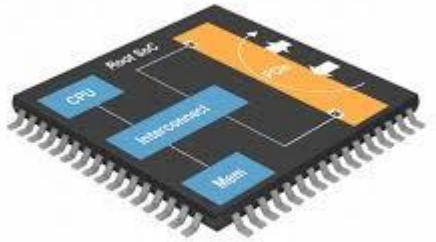
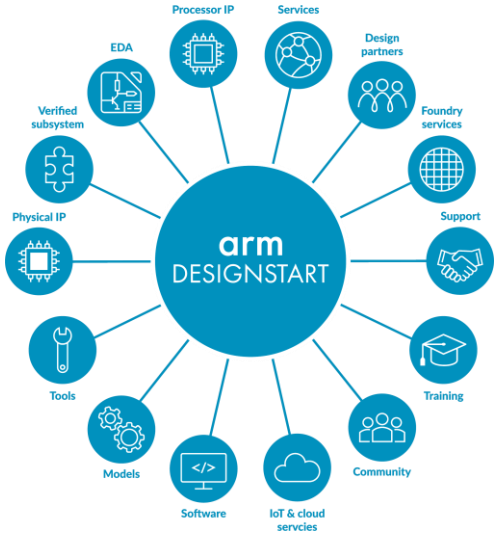
# Current Research Enablement Portfolio

- SoC building blocks
  - HW IP - CPUs, Interconnects, other peripherals*
  - Physical IP - Standard cells, Memory compilers, POP IP
  - Tools and SW - DS-5, mbed OS, compute library, CMSIS-NN, etc




- Reference HW systems and integrated SW packages (DesignStart)
  - Cortex M0/ M3 based systems, evaluation with obfuscated RTL (DesignStart Eval)
  - Cortex M0/ M3 based systems, RTL for SoC design (DesignStart Pro Academic)
  - FPGA optimised cores Cortex M1/ M3 (DesignStart FPGA)
  - Cortex M33 based system, HW/SW codesign in the cloud (DesignStart FPGA on Cloud – AWS F1 instances)


- Compute systems modelling and architecture exploration
  - Gem5 - CPU and system modelling
  - Fast models and Fixed Virtual Platforms (FVP) – functional SW prototyping




*Any logic Arm IP that is not part of DesignStart will be provided on a case by case basis, depending on the research project scope, objectives and alignment with Arm research agenda

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# Arm Foundry Partners

## In discussions with Europractice and MOSIS to help you further accelerate your silicon tape out

**Physical IP Available in DesignStart:**

★ = Fee-based ★ = Mixed ★ = Free **Highlighted Cell** = Need approval from Foundry

| Company | 16/14 nm FinFET | 20 nm | 32 nm 28 nm | 45 nm 40 nm | 55 nm | 65 nm | 80 nm | 90 nm | 110 nm | 130 nm | 150 nm | 160 nm | 180 nm | 250 nm |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSMC | ★ | ★ | ★ | ★ | ★ | ★ | ★ | ★ | ★ | ★ | ★ | ★ | ★ | ★ |
| GLOBALFOUNDRIES | ★ | | ★ | | ★ | ★ | | ★ | | ★ | | | ★ | ★ |
| IBM (GF FI) | ★ | ★ | ★ | ★ | | ★ | | ★ | | ★ | | | ★ | |
| Samsung | ★ | ★ | ★ | ★ | | ★ | | ★ | | | | | | |
| UMC | | | ★ | ★ | ★ | ★ | | ★ | | ★ | | | ★ | |
| SMIC | | | ★ | ★ | | ★ | | ★ | ★ | ★ | | | ★ | |
| Hynix | | | | | | | | ★ | | | | | ★ | |
| SilTerra | | | | | | | | | ★ | ★ | ★ | | ★ | |
| CSMC | | | | | | | | | | ★ | | | | |
| Dongbu | | | | | | | | | | ★ | | | ★ | |
| Tower-Jazz | | | | | | | | | | ★ | | | ★ | |
| HeJian | | | | | | | | | | | | ★ | ★ | |
| XMC | | | | | ★ | | | | | | | | | |
| Grace → HHGrace | | | | | | | | | | | | | ★ | |
| HHNEC → HHGrace | | | | | | | | | | | | | ★ | |
| XFab | | | | | | | | | | | | | ★ | ★ |
| MagnaChip | | | | | | | | | | | | | ★ | |
| Vanguard | | | | | | | | | | | | | ★ | ★ |

EUROPRACTICE

MOSIS



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# Arm Research Enablement Examples

Wide range of Arm IP available for a range of research projects

## Human Brain Project

- EU funded project to develop neuromorphic chips
- 144x Arm Cortex M4 included in SpiNNaker-2 prototype chip

## Euro Exa


- EU funded project to develop Exa-scale HPC
- Arm Cortex A73 based subsystem is the core building block

## High Performance Spaceflight Computing


- NASA-funded project
- Bringing cutting edge processor technology to space applications
- Arm Cortex A53-based, radiation-hardened SoC

## Mont Blanc


- EU funded HPC project
- 3x 3Y projects delivered 2 prototypes
- Powered by Cavium ThunderX2 Armv8 processors

## Uniserver


- Universal micro-server ecosystem development
- Powered by Applied Micro Armv8 processors

## Advanced Technology Benchmarking


- Co-optimisation of advanced process nodes and state of the art designs
- Based on Arm Cortex A53



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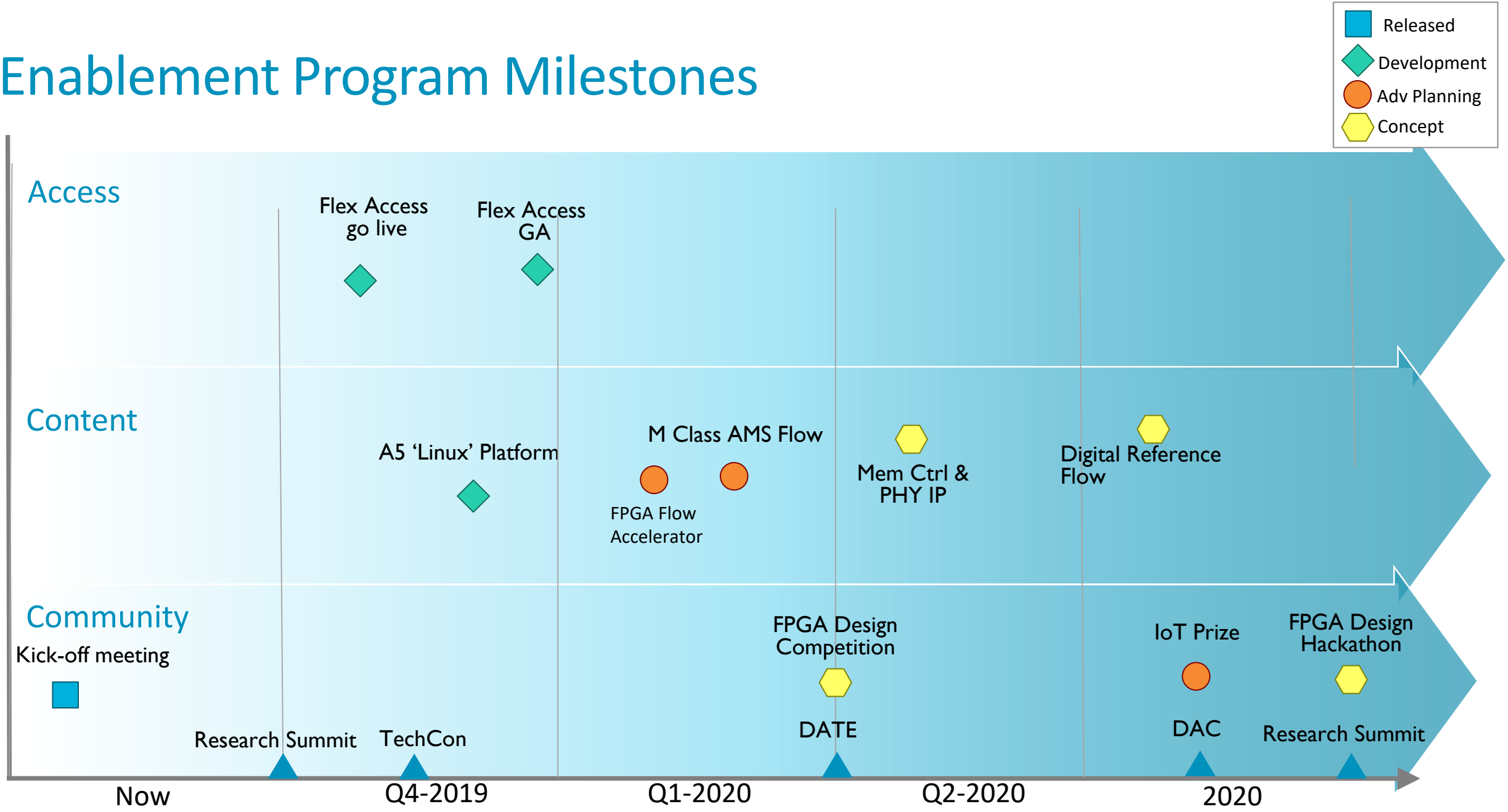
# Enablement Program Milestones



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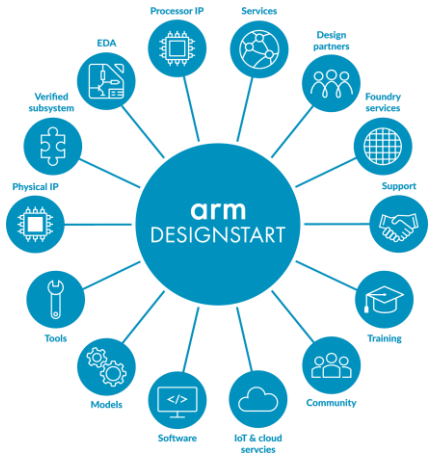
# Arm Research Enablement: New Initiatives

# Arm RE New Key Initiatives Announced

## Cortex-A5 addition to DesignStart Pro Academic

- First DesignStart subsystem supporting Linux and other rich OSs



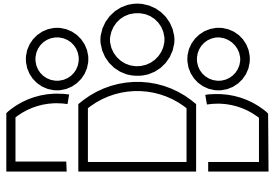

## Arm Flexible Access for Research

- Simplified distribution of extended Arm technology portfolio
- Subscription-based model, aligned with AFA commercial scheme

**Open Access**

## Arm Research SoC Labs

- New, open community to facilitate academic SoC/SoFPGA devel opment
- Increasing our investment to support the community





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# Arm Flexible Access for Research

# Arm Flexible Access for Research program

## Wider range of IP

- Access wide range of Arm IP for research purposes
- Complete RTL for cores and subsystems

## Simplified, quicker process

- Speed-up the approval process from several weeks or months to **two days**
- Subscription based model

## Simplified legal framework

- Reduce friction with **simple** click-through End-User License Agreement (EULA)



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# Arm Flexible Access for Research IP portfolio

| Cortex-A High Performance CPUs |
| --- |
| Cortex-A5 |
| Cortex-A7 |
| Cortex-A32 |
| Cortex-A34 |
| Cortex-A35 |
| Cortex-A53 |
| All with support for Neon/FPU/ETM |

| Cortex-R Real Time CPUs |
| --- |
| Cortex-R5 |
| Cortex-R8 |
| Cortex-R52 |
| All with support for Neon/FPU/ETM |

| Cortex-M Efficient Embedded CPUs |
| --- |
| Cortex-M0 |
| Cortex-M0+ |
| Cortex-M23 |
| Cortex-M3 |
| Cortex-M4 |
| Cortex-M33 |
| Cortex-M7 |
| Support for FPU/ETM/MTB |

| Corstone Foundation IP |
| --- |
| Corstone-201 |

| Design Start |
| --- |
| Cortex-A5 DesignStart Academic Pro |

| Mali Graphics |
| --- |
| MALI-G31 |
| MALI-G52 |
| Support for with Android/Linux DDK |

| IP Tools |
| --- |
| Socrates IP configuration Tool |

| CoreLink Peripherals |
| --- |
| CoreLink CCI-550/NIC-450 Interconnect |
| CoreLink L2C-310 L2 cache controller |
| CoreLink DMA-330/230 DMA controller |
| CoreLink GIC-500 Interrupt controller |
| CoreLink MMU-500 system MMU |
| CoreLink Peripherals (UART, GPIO etc) |

# Arm Flexible Access for Research IP portfolio

| CorStone 201 Foundation IP |
| --- |
| CM0SDK / CMSDK peripherals |
| AHB Flash Cache |
| TRNG |
| RTC |
| CoreLink SIE-200 System IP |
| LPD-500 (Low Power Distributor) |
| CoreLink GFC-100 Flash Controller |
| CoreLink GFC-200 Flash Controller |
| PCK-600 Kratos (power control) |
| SDC-600 Chaucer (authenticated debug) |
| SSE-050 subsystem (Cortex-M3) |
| SSE-200 subsystem (Cortex-M33) |
| Arm Cortex-M0/M0+ Example System |

| CoreSight Debug |
| --- |
| CoreSight SoC-400 Debug and Trace |
| CoreSight SDC-600 Secure Debug Channel |
| CoreSight STM-500 System Trace Macrocell |
| CoreSight System Trace Macrocell |
| CoreSight Trace Memory Controller |

| Software Tools |
| --- |
| ARM Development Studio |
| IDE debugger |
| Streamline performance Analyzer |
| Arm Complier |
| Software packs (device drivers, middleware etc.) |
| Arm Fixed Virtual Platforms |
| Arm Cycle Models |
| Arm Fast Models |

# Academic Use Cases Unlocked

## System design to support specific research applications/topics

- Accelerators and SW for specific use cases, peripherals, analog circuits

## System design to support system architecture research

- Heterogenous subsystems design, focus on accelerator topology, cache hierarchy, NoC technologies, system security features, etc

## System design to support design methodology research

- New system design methodologies, tools and flows

## Physical design technologies research

- Arm IP or system used for optimisation

# Arm Flexible Access for Research: Legal Framework

- Subscription license model
  - One legal agreement to access the whole IP portfolio
- Terms related to physical secure rooms, enhanced IT security policy or external auditing are removed
  - We only require a yearly project review report, to explore collaboration and understand how our technology is being used
- IP feedback clauses and non-exclusive royalty free rights to new technologies developed on top of Arm IP removed
  - We encourage open sourcing new technologies, but not asking for NERF rights to research results
  - Easier to collaborate with academia
- Processor modifications not permitted for now
  - Gem5 is a great option for processor and system architecture exploration



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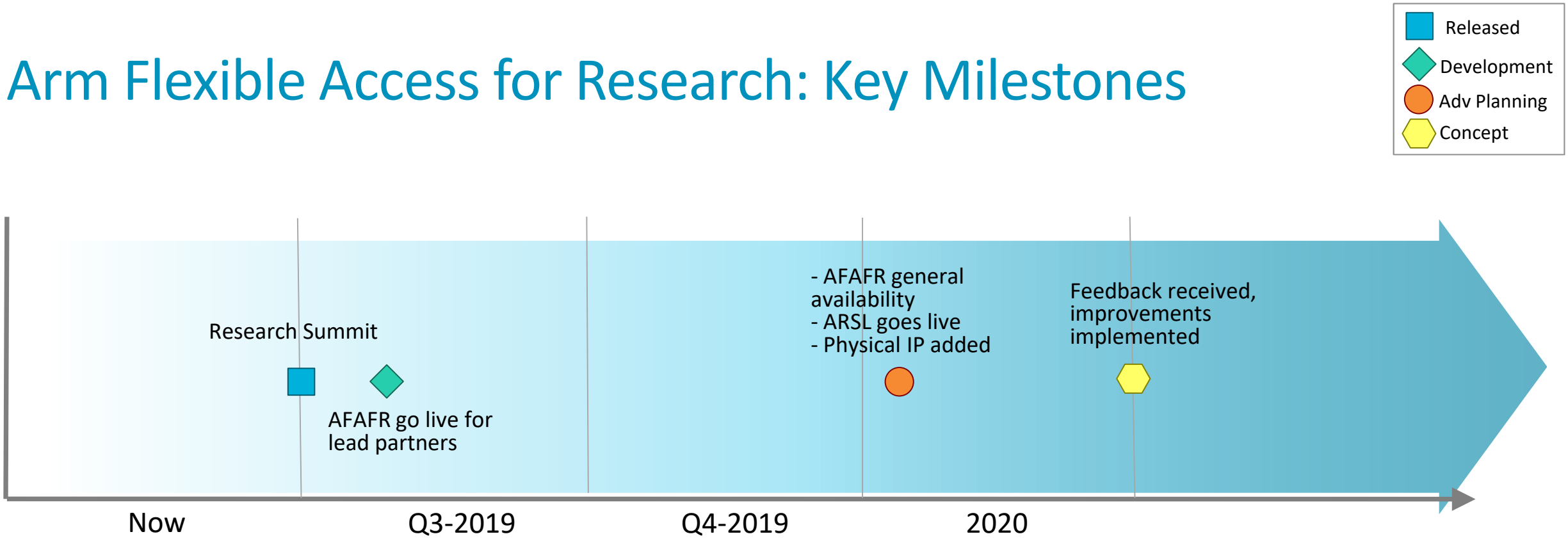
# Arm Flexible Access for Research: Key Milestones




- September'19: Announce Arm Flexible Access for Research and Arm Research SoC Labs at Research Summit
- October'19: Arm Flexible Access for Research go live, available to lead partners
- Q1'20: Arm Flexible Access for Research general availability and Arm Research SoC Labs go live
  - Adding Arm physical IP to Arm Flexible Access for Research
  - Arm Research SoC Labs goes live
- Later in 2020: Arm Flexible Access for Research incremental improvements



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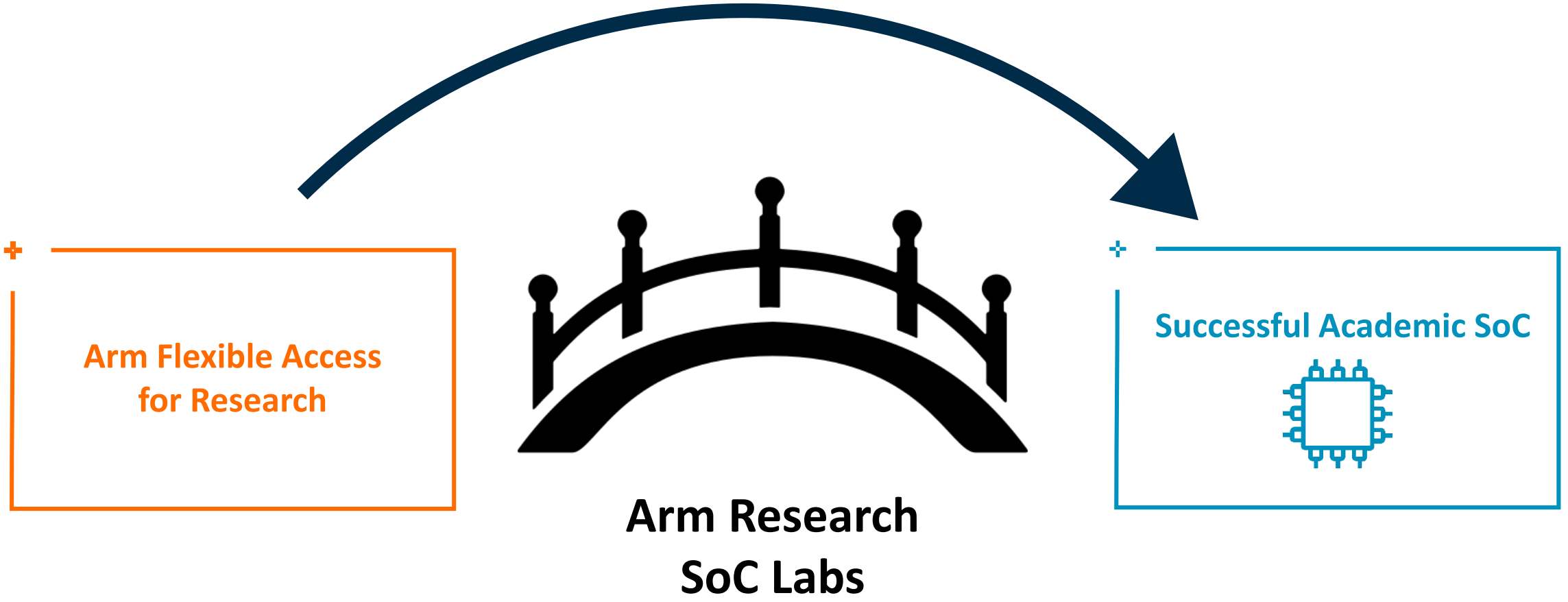
# Arm Research SoC Labs

# Why do we need Arm Research SoC Labs?



# Arm Research SoC Labs: A Distributed Community

Arm Research SoC Labs is a distributed academic community with some common reference points:

- Access to the same Arm IP
  - Provided by Arm Flexible Access for Research
- Arm Research SoC Labs portal for:
  - Promotion of technical deliverables created by SoC Labs contributors
  - Arm commercial partner's offerings to academic research
- Regular conferences to strengthen the community and discuss:
  - New technology trends and hot research topics
  - Gaps in SoC labs ecosystem and suggestion to address them
  - Joint bids for government funded research projects

# The Arm Research SoC Labs Portal

- The Arm Research SoC Labs portal is an index to academic and commercial offerings
  - Arm doesn’t intervene or dictate the delivery channel – each contributor uses their own
  - Arm doesn’t take ownership of collateral provided
- SoC Labs portal underpins academic collaboration and knowledge sharing
  - No Arm access control to SoC Labs portal – available to everyone!
- Arm IP cannot be redistributed on the SoC Labs portal
  - Working on the methodology to replace Arm IP with dummy files



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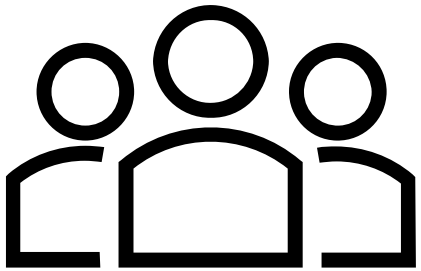
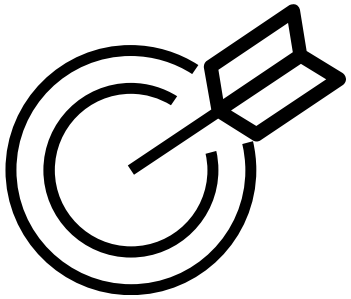
# Why should you contribute to Arm Research SoC Labs?

Actively contributing to Arm Research SoC Labs opens up a number of benefits



Closer collaboration with Arm Research

Opportunities to promote your research to world class conferences along with Arm



Gain more visibility and recognition among your research peer group



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# Arm Research Enablement Kits

- Arm actively invests in creating additional infrastructure technologies to facilitate research
  - All collateral to be referenced in Arm Research SoC Labs portal
- Arm Coherent Accelerator Interface
  - Cache coherency between Arm processors and accelerators
- Prototyping on AWS F1 instances
  - M33 based system available on AWS marketplace
  - RTL wrappers to be provided to help with porting any Arm subsystem to the F1 instances

Thank You
Danke
Merci
谢谢
ありがとう
Gracias
Kiitos
감사합니다
धन्यवाद
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