Simplifying Linux-capable silicon designs with Arm DesignStart

September 2019

Cortex-A5 DesignStart Academic

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Arm DesignStart Academic: Free and Easy access to Arm IP for custom silicon designs

	Cortex-M0 DesignStart Academic	Cortex-M3 DesignStart Academic
IP Package	• Cortex-M0 • Cortex-M System Design Kit	• Cortex-M3 • Cortex-M System Design Kit • CoreLink SSE-050 Subsystem • AHB Flash Cache • True Random Number Generator • Real Time Clock
Out-of-box software support	• Bare metal test examples	• Mbed OS • Bare metal test examples
FPGA prototyping	Arm MPS2+ board	

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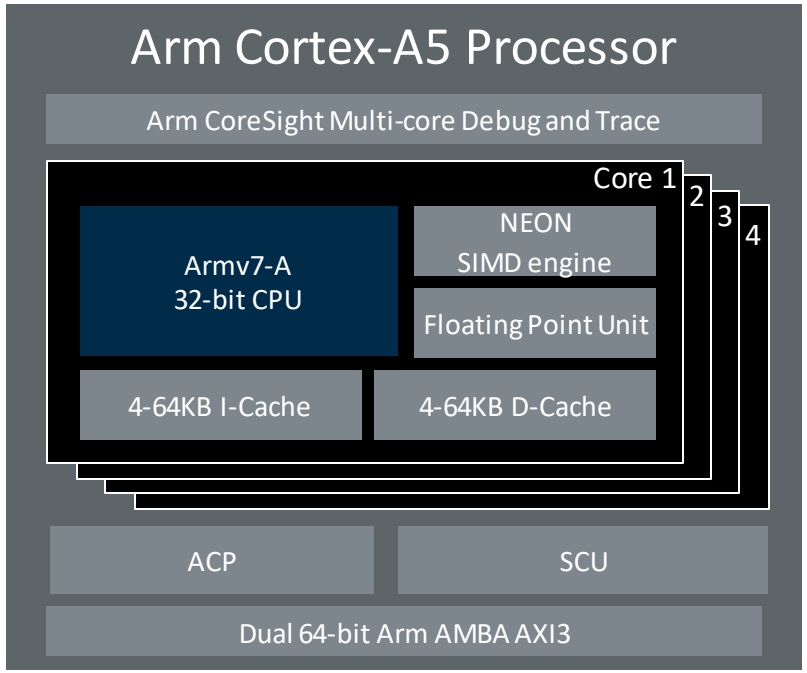
Cortex-A5: High Performance and Efficiency, Fully Featured CPU



Scalable GHz performance

High Performance, advanced CPU

- ✓ Up to 4 CPUs for maximum performance
- ✓ Coherency for easy data sharing
- ✓ Advanced data processing with SIMD engine

Ultra-high efficiency

- ✓ Smallest area for advanced CPU

Easy integration of accelerators

- ✓ High performance Advanced Accelerator Port (ACP) for fast connection to ML and custom accelerators

Hardware security with Arm TrustZone

- ✓ Industry-proven security built in the CPU

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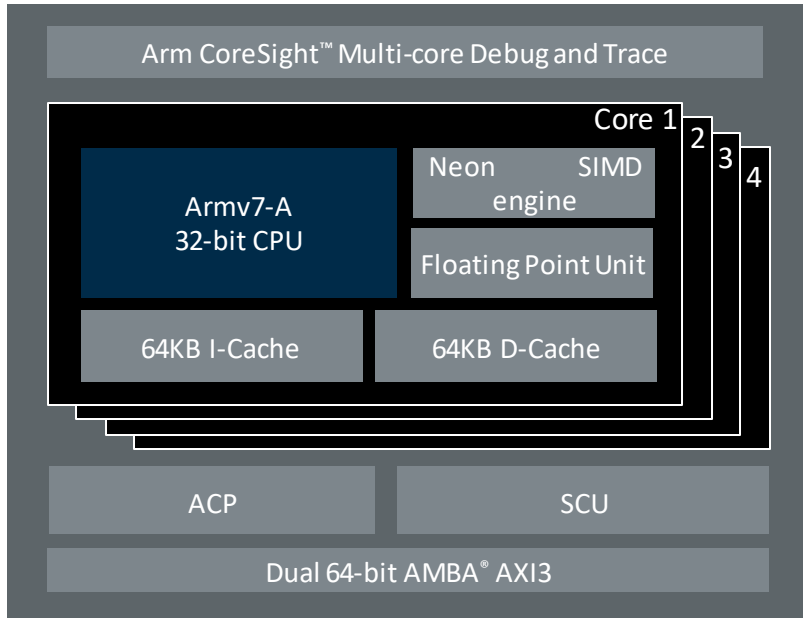
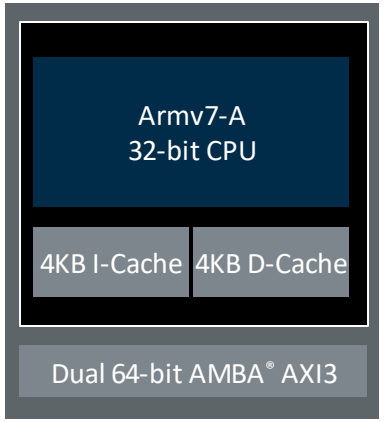
Highly Configurable for Diverse Embedded Applications

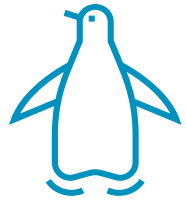
Performance-optimized multi-core configuration



Rich IoT gateway

Area-optimized configuration





Linux and RTOS-capable

Minimal footprint (0.28 mm^2)

Highest energy efficiency (10mW/100MHz)

Deeply embedded controller

Dhrystone

Total power reported at typical operating conditions, Process – 40LP

Cortex-A5 DesignStart: Simplifying Linux-capable silicon design

Upcoming release

Currently available

Comprehensive package

- Cortex-A5 with Neon media processing engine
- Configurable AXI Interconnect
- L2 Cache controller
- Debug and Trace module (CoreSight)
- SRAM controller
- Watchdog, Timer, UART
- General Purpose I/O peripheral
- Real Time Clock
- True Random Number Generator (TRNG)
- Interconnect configuration tool

Subsystem ★

Pre-validated and configurable reference design to reduce design complexity

Simulation Models ★

Start software development before hardware is available to shorten development time

Linux port ★

Take advantage of open-source software with out-of-the-box Linux support

FPGA prototyping ★

Prototype your designs on an Arm MPS3 FPGA prototyping board

★ New features to be added in upcoming release

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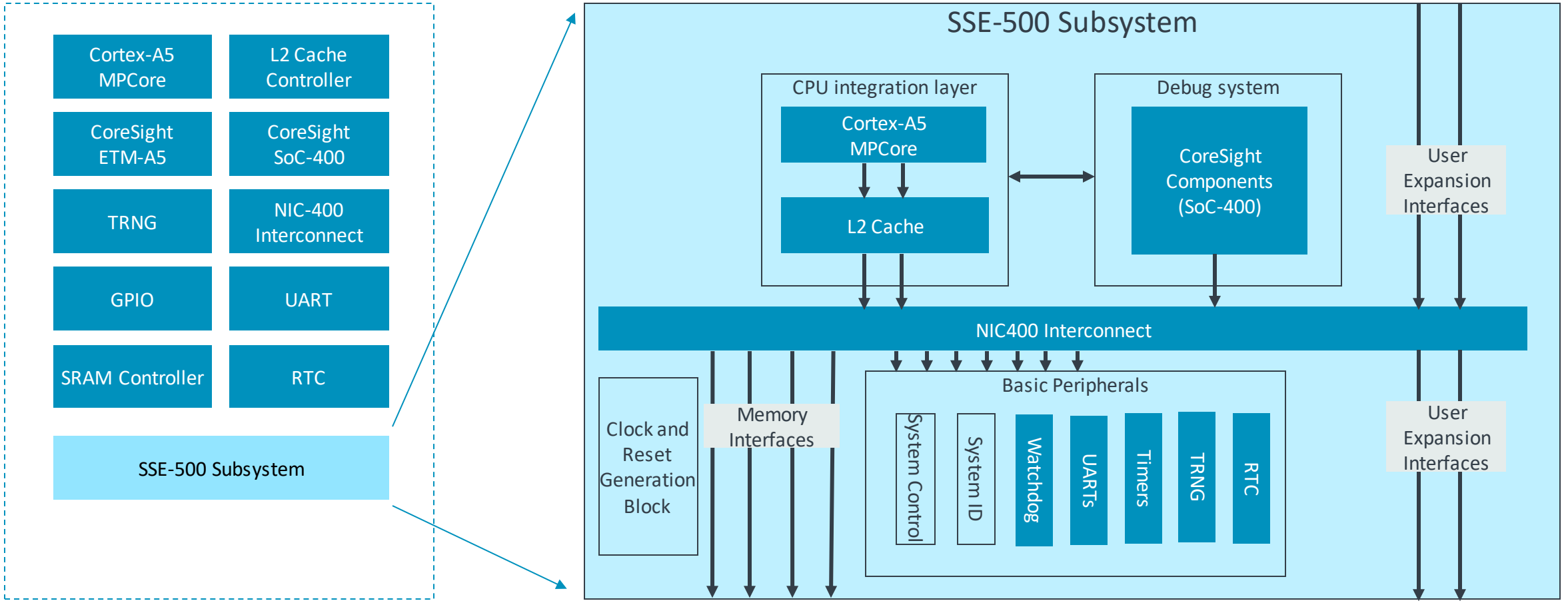
SSE-500 Example Subsystem: Proven Foundation for Your Custom Silicon Designs



DesignStart IP package

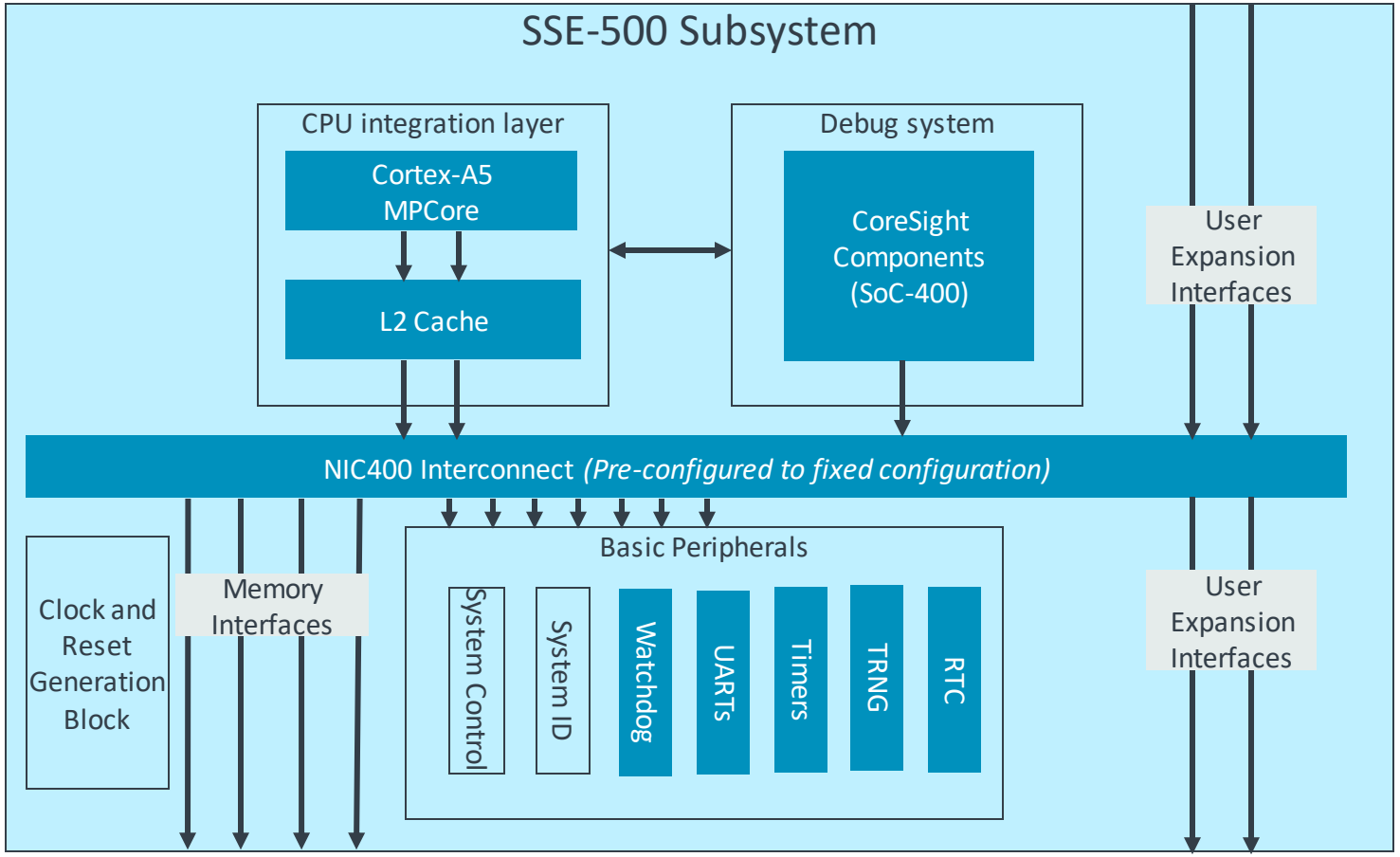
Pre-verified and pre-integrated by DesignStart, and easily configurable as per design needs

Simplifying Interconnect Configuration Challenges

NIC-400 User expansion ports

User expansion ports

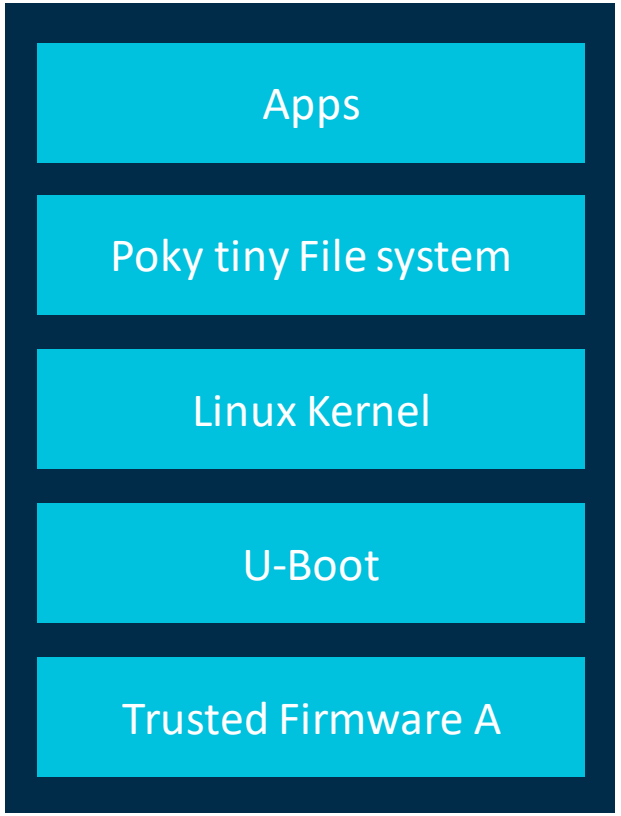
- 4 expansion ports available
- Additional IP can be connected into these
- Reduce the need for reconfiguring the NIC-400
- Documents and scripts available for designs that need to reconfigure NIC-400
- L1 I/D Cache 16KB, L2 Cache 128KB



Take Benefits of Extensive Open-source Support for Arm

Out-of-box basic Linux port included in the package

- Trusted Firmware A with Armv7 support, offering a foundation for adding security features
- U-Boot with generic Timer support
- Linux kernel support enabling access to extensive open-source repository
- Yocto based poky-tiny distro support for easy build, distribute and deployment
- Complete Software with build and fetch instructions will be available through community pages



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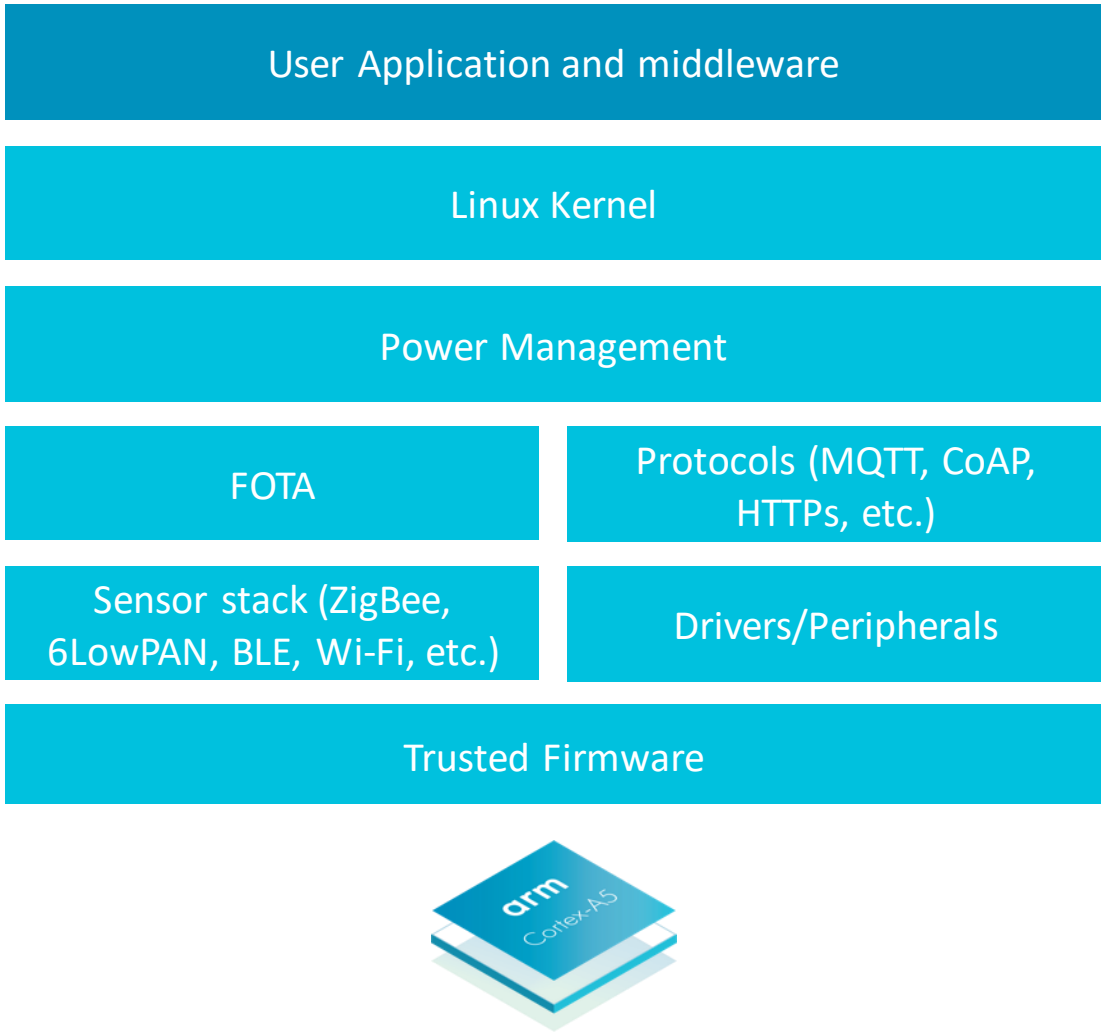
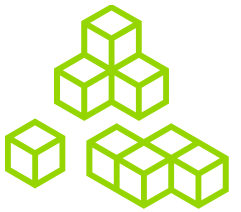
Linux on Arm: Industry-proven for IoT Applications





Widest choice of middleware projects developed for Arm

Widest choice of supported software drivers and frameworks

Optimized firmware for easier security and power efficiency

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Simulation Models

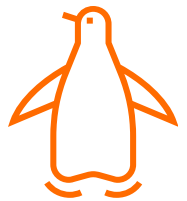
Simplified performance analysis and software development using Arm models

Arm Cycle Models

- 100% Cycle Accurate models for Cortex-A5 performance evaluation
- Software model environment gives greater visibility of bottlenecks and shortens debug time
- Quickly explore configuration space to identify optimal performance profile

Arm Fast Models

- Fast, functionally accurate models enable software development in the absence of hardware
- Virtual platform with reference Linux port for rapid software development



Cortex-A5 DesignStart: Release Timeline

Currently available
Cortex-A5 CPU IP & System IP package

Q4 2019
Fast Model of DesignStart package including SSE-500 subsystem and Linux port

Q1 2020
RTL availability of DesignStart package including SSE-500 subsystem and Linux port

Q2 2020
FPGA prototyping on MPS3 board for the DesignStart package

Thank You
Danke
Merci
谢谢
ありがとう
Gracias
Kiitos
감사합니다
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Back-up