

A Self-Tuning Cortex-M0 IoT Processor Based on Leakage-Ratio Measurement for Energy-Optimal Operation

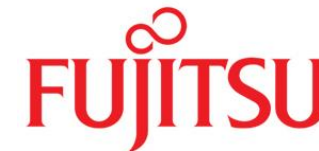
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Motivation: IoT Is Everywhere

- ❑ Wireless sensors for IoT

- Power-constrained → **Efficient energy consumption**

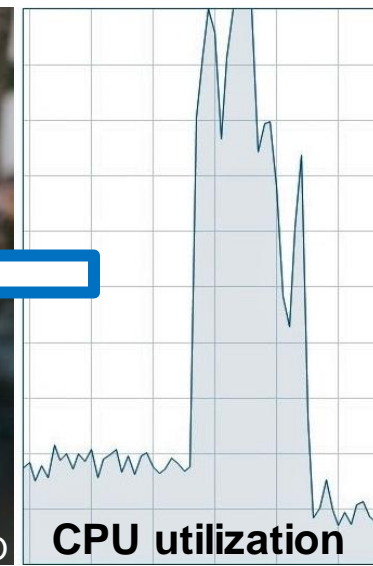
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- Wide range of environments → **Runtime adjustment**
 - ✓ Various temperatures & performance requirements



<Various temperatures>



<Various performance requirements>

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 - ✓ Various temperatures & performance requirements

➔ **Goal: Runtime adjustment** for energy efficiency
across a wide range of
Process & Temperature & Performance goals

<Various temperatures>

Photo credit: AcuRite.com

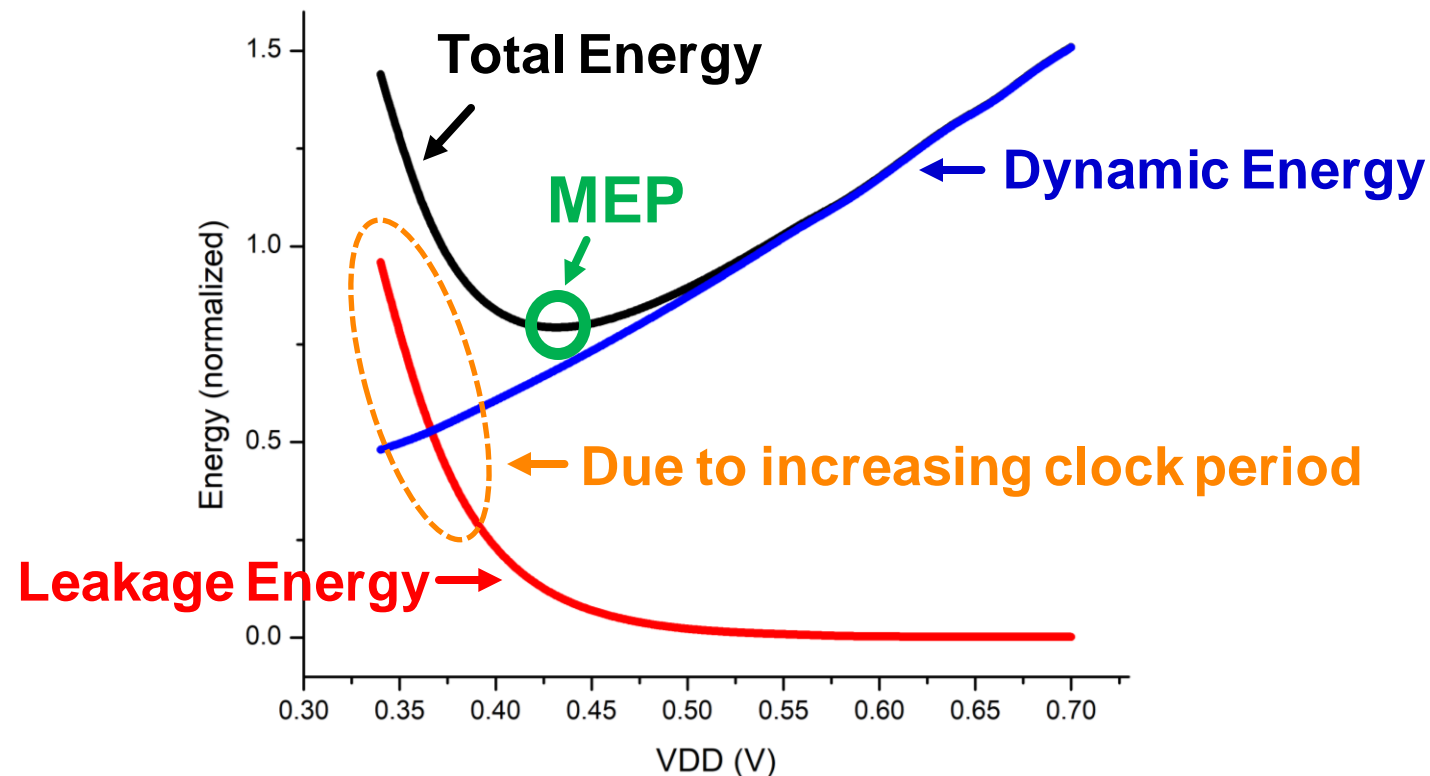
Photo credit: ALRO

CPU utilization

<Various performance requirements>

Background: Minimum Energy Point (MEP)

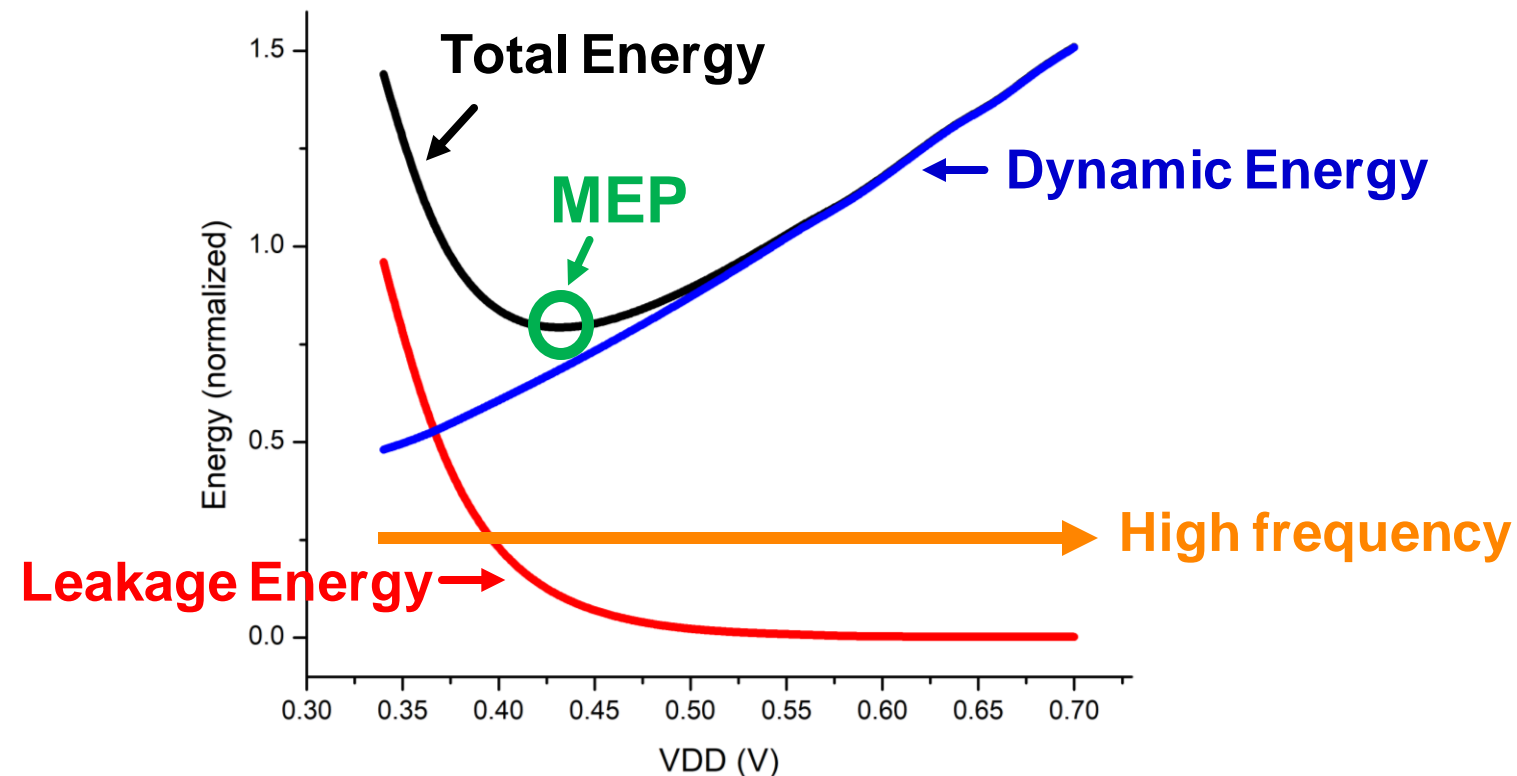
- MEP: VDD at which total energy per operation is minimum
 - Total energy = Dynamic energy + Leakage energy



Goal: Runtime MEP Tracking

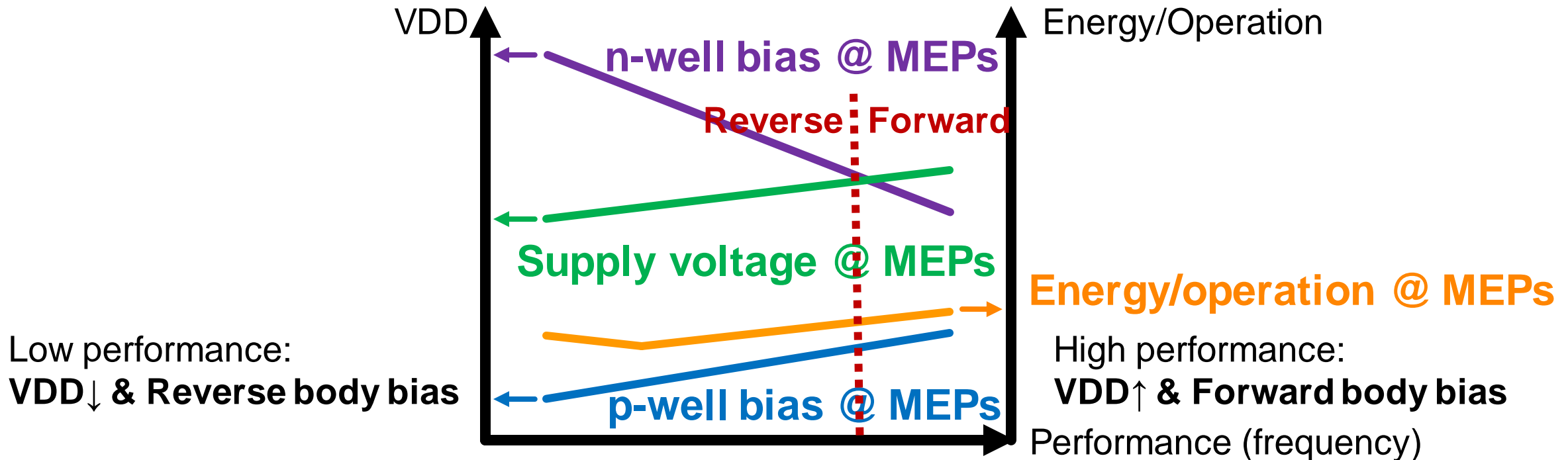
- ❑ Run the circuit at MEP

- Adaptive supply voltage: Results in a **single** MEP-performance point



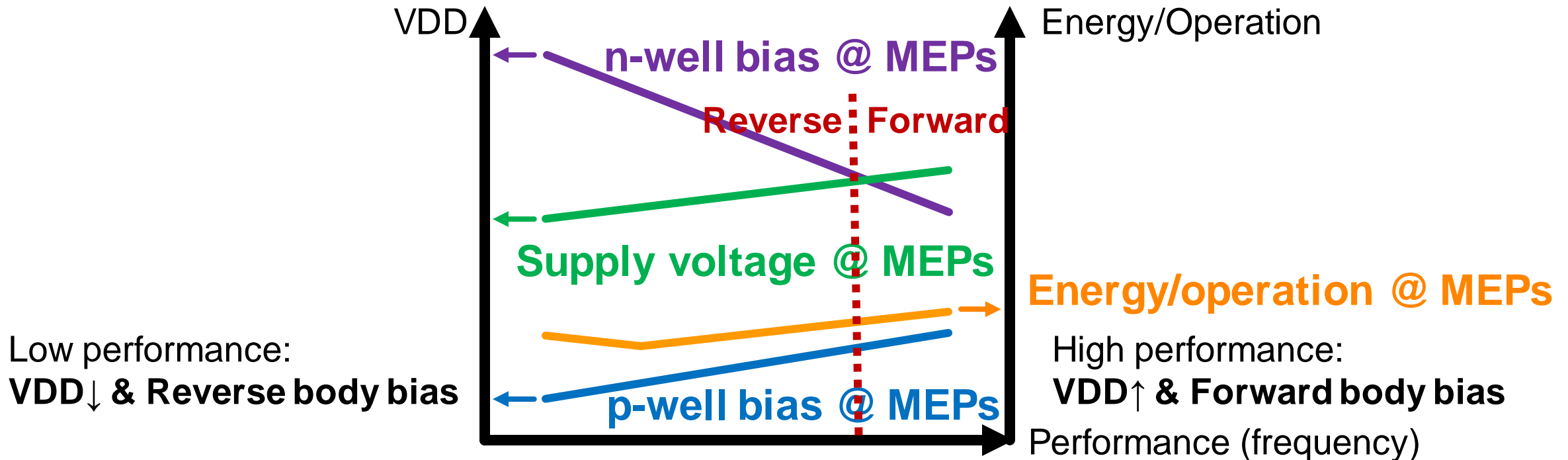
Goal: Runtime MEP Tracking

- ❑ Run the circuit at MEP
 - Adaptive supply voltage
 - Adaptive body bias: Results in **multiple** MEP-performance points



Goal: Runtime MEP Tracking

- ❑ Run the circuit at MEP
 - Adaptive supply voltage
 - Adaptive body bias: Results in **multiple** MEP-performance points
 - ✓ Benefit from DDC process (large body coefficient)

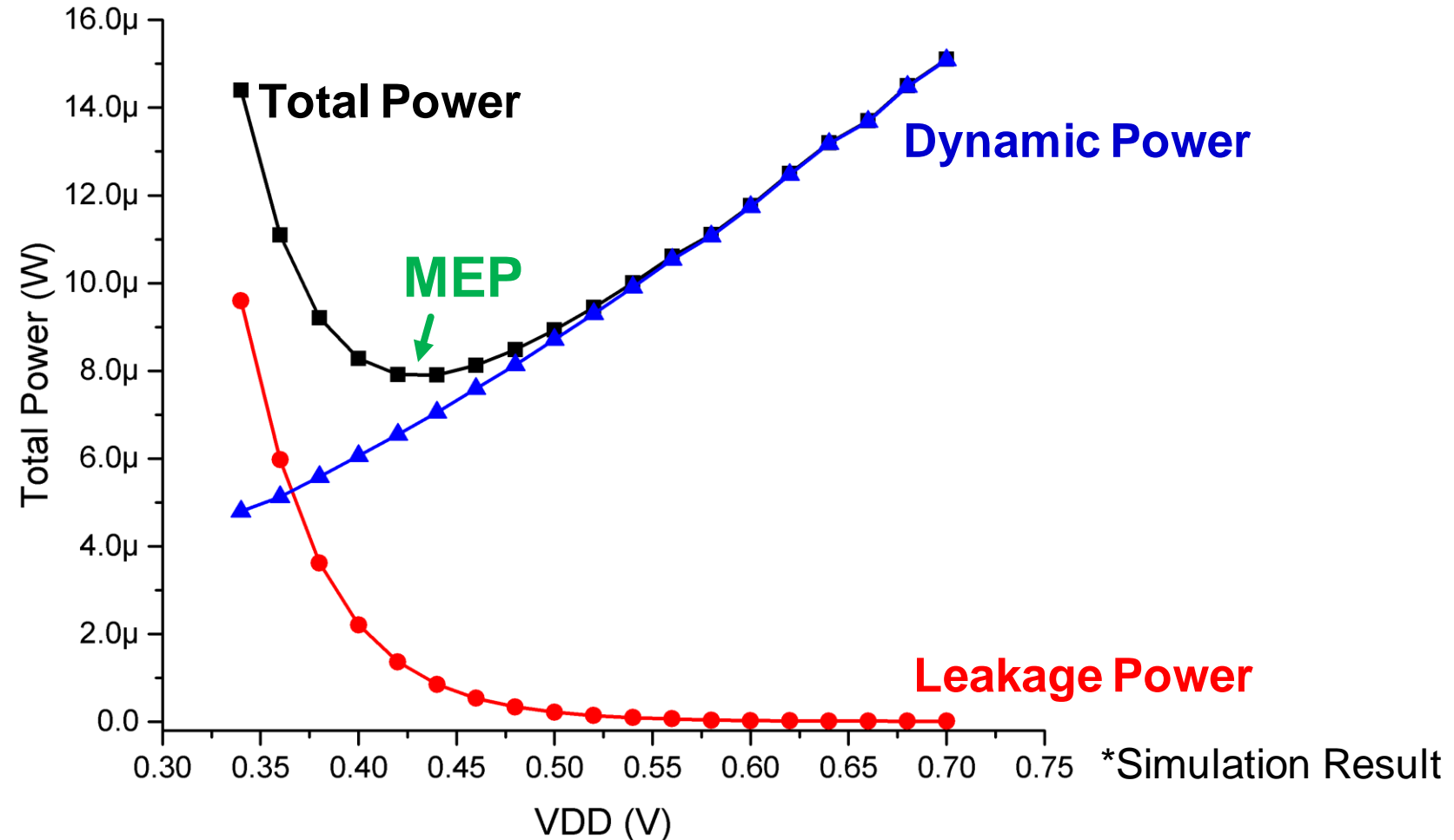


Challenge: Runtime MEP Tracking

- ❑ Need to find MEP without system halt or reset, and significant hardware/power overhead

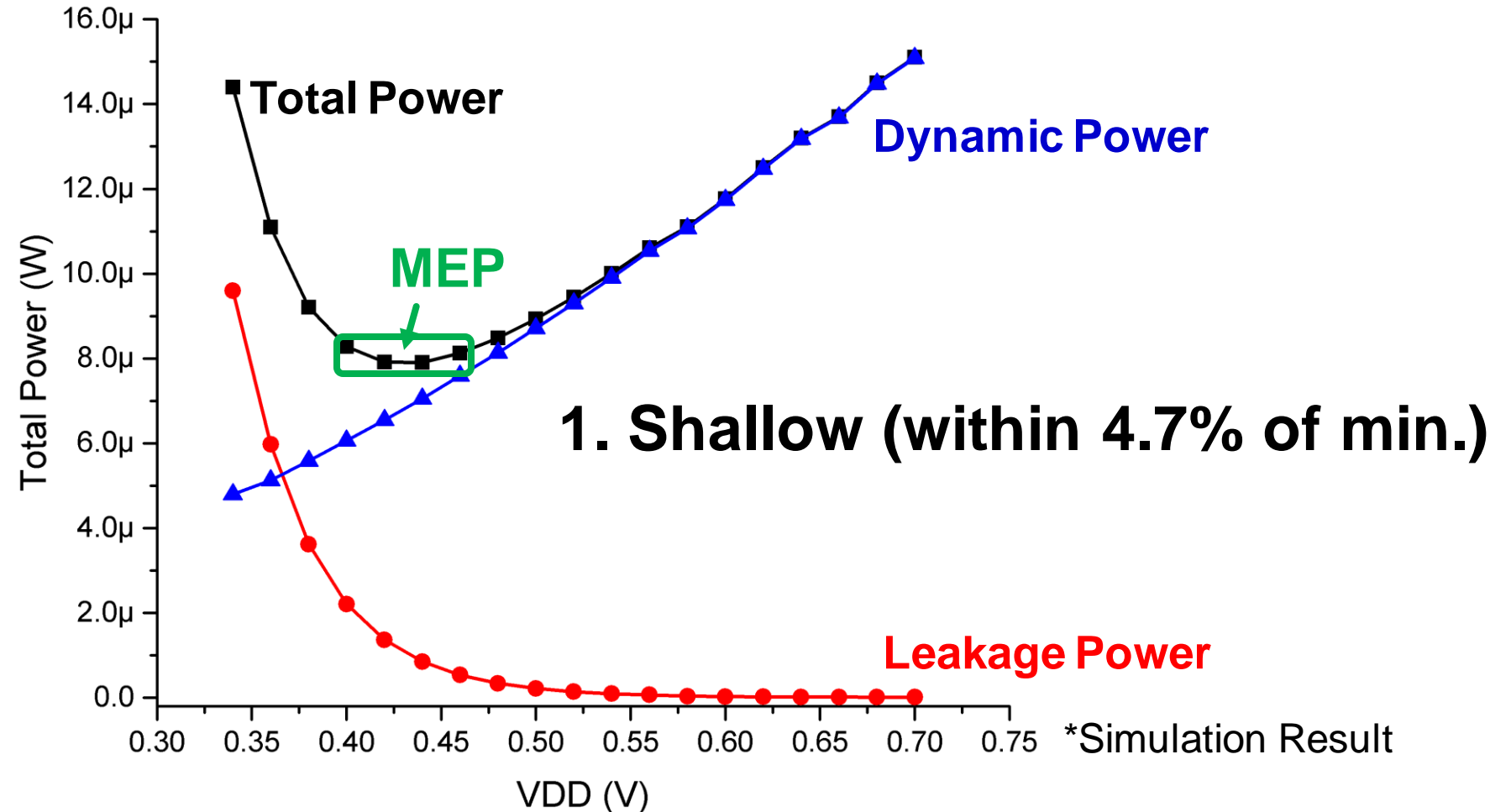
Key Observation: Optimal Leakage Ratio

- Fixed frequency: Total power = Dynamic power + Leakage power



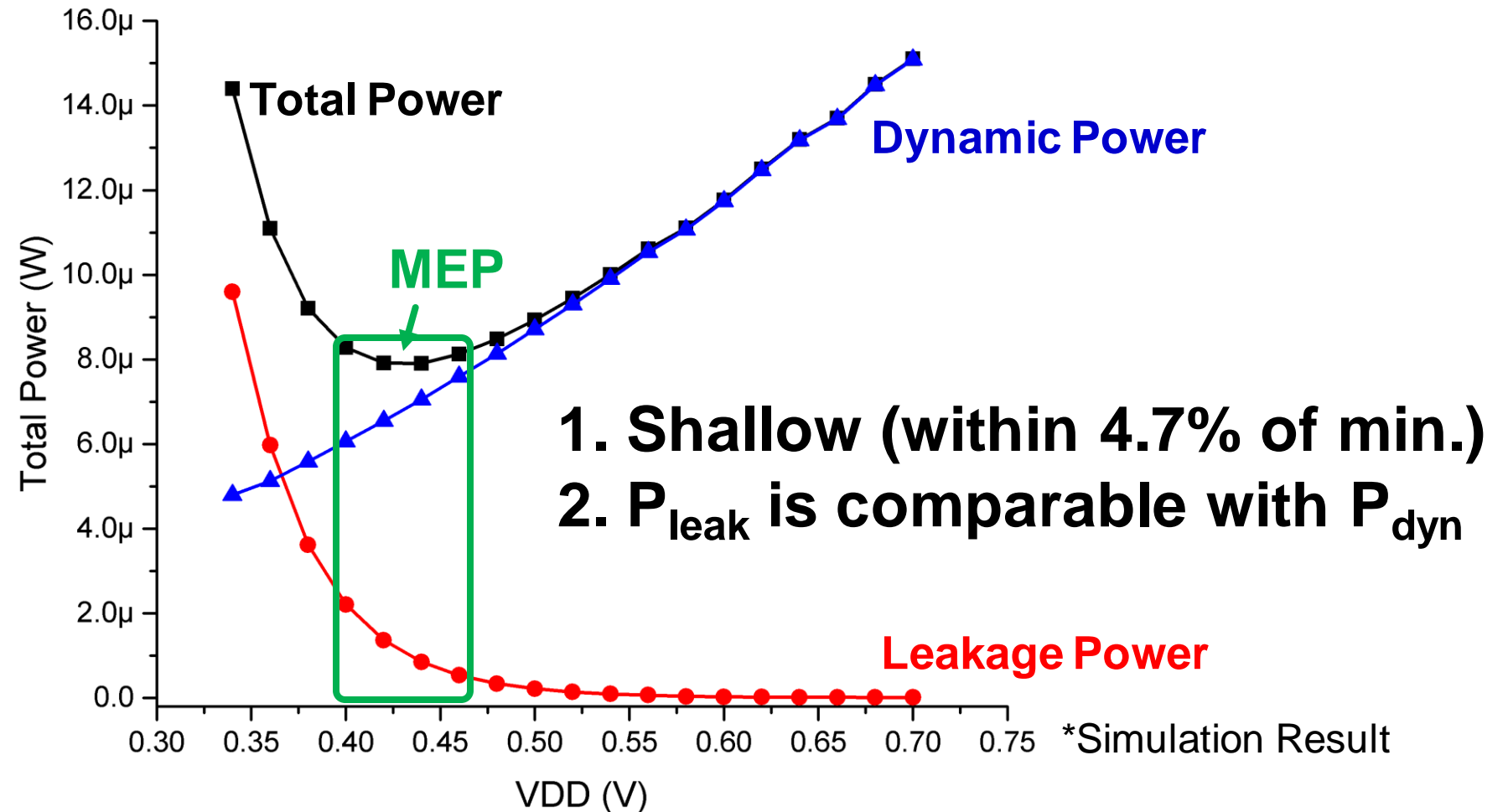
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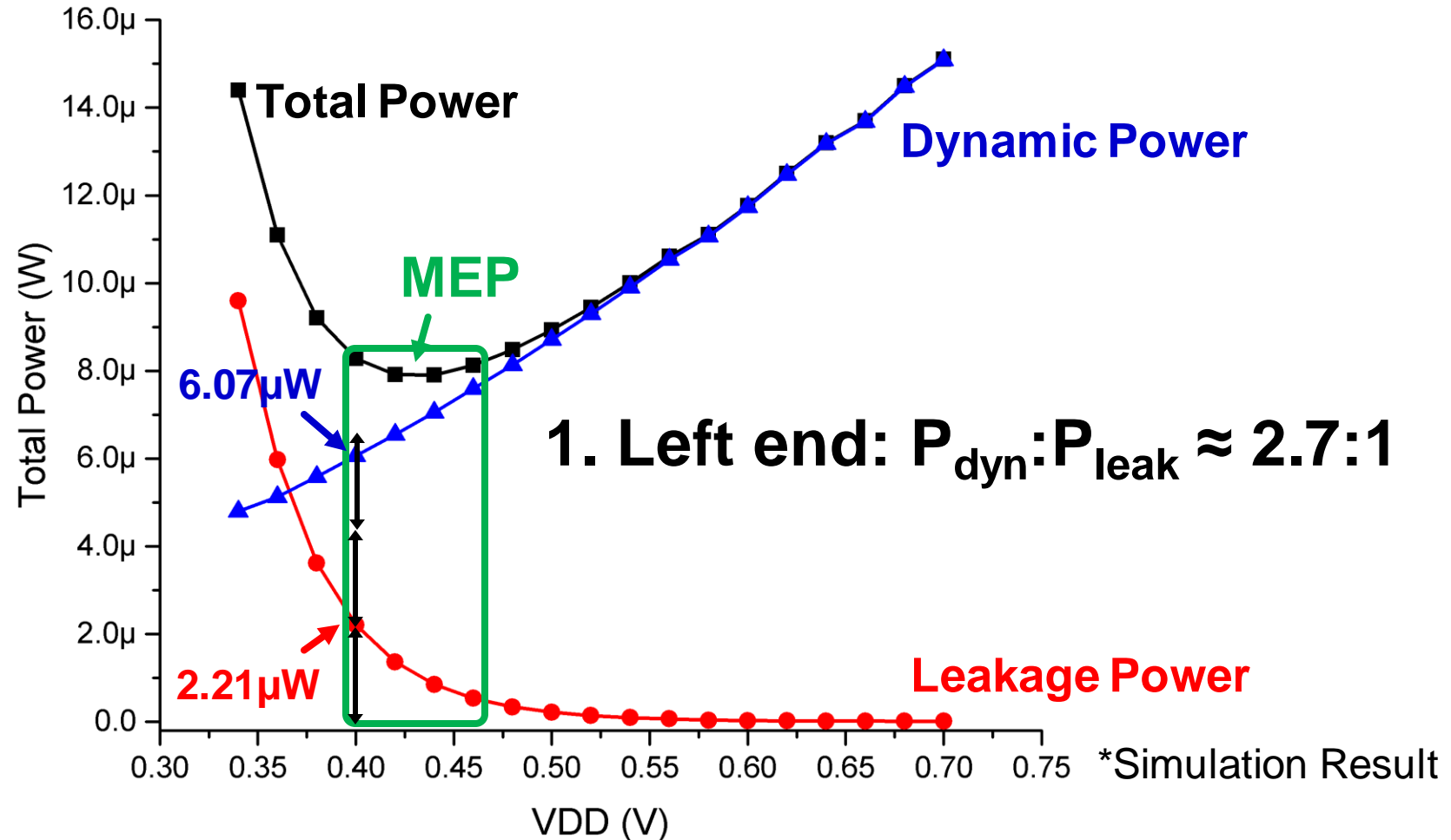
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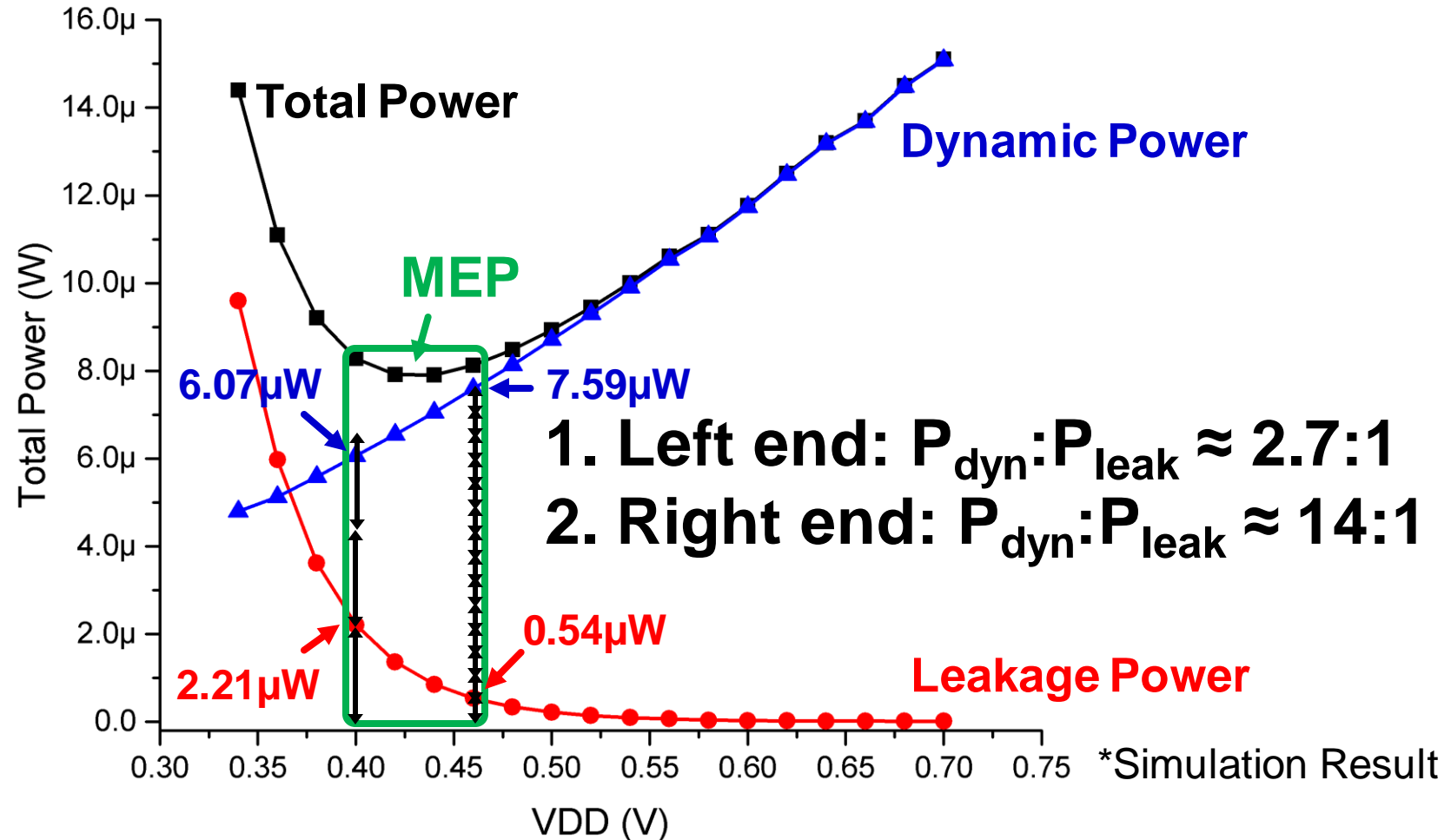
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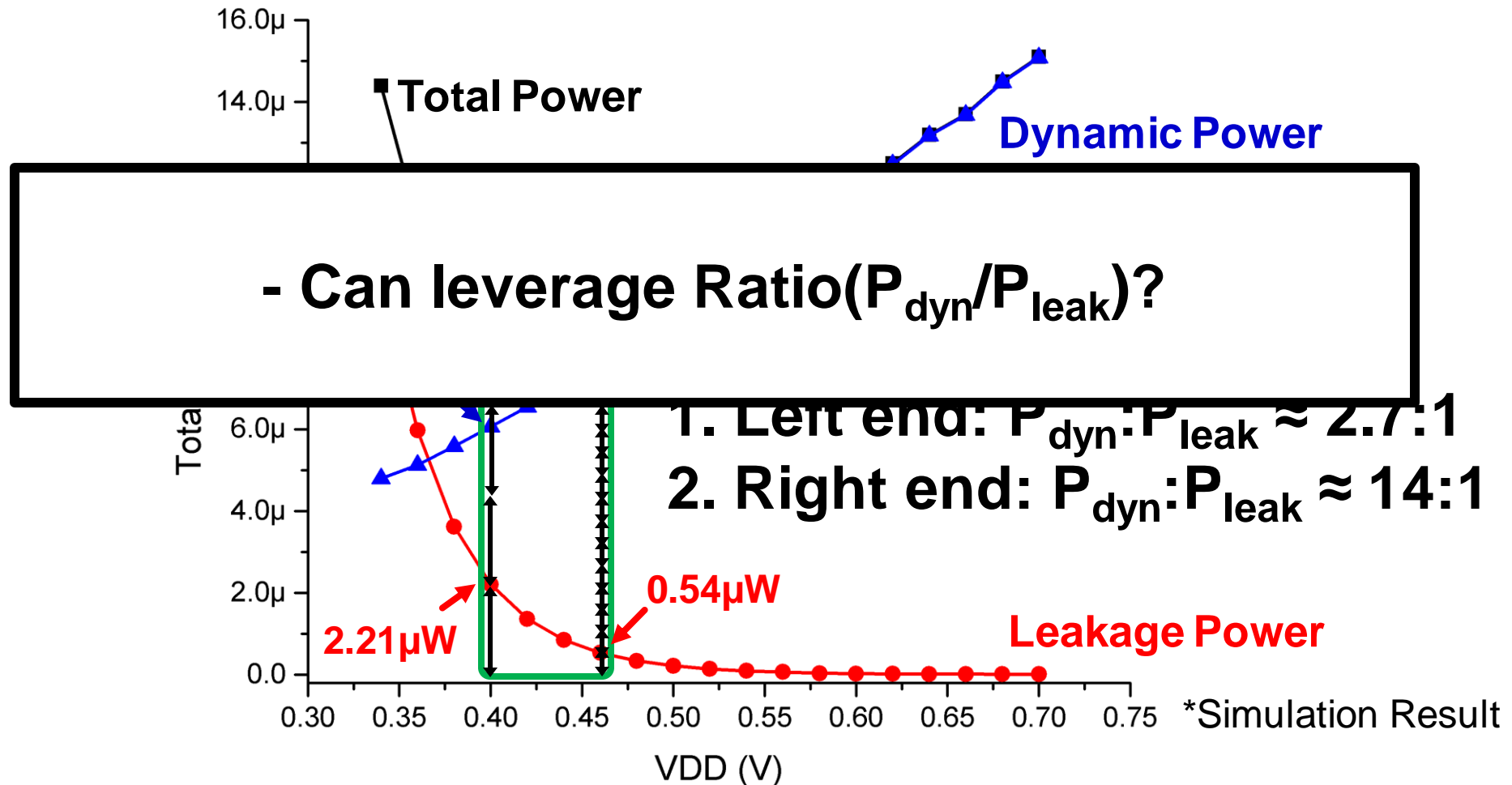
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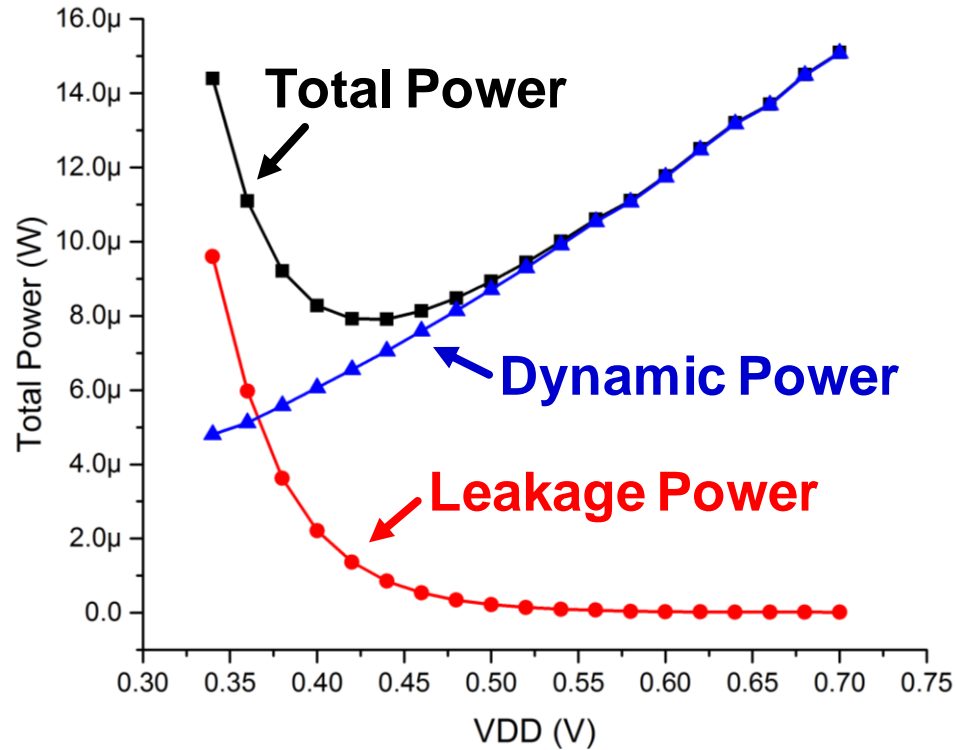


Key Observation: Optimal Leakage Ratio

□ Derivation of optimal leakage ratio

*Simulation Result (Under fixed Frequency)

Assume $P_{leak} = aV_{DD}^{-b}$ (a, b is *const.*)

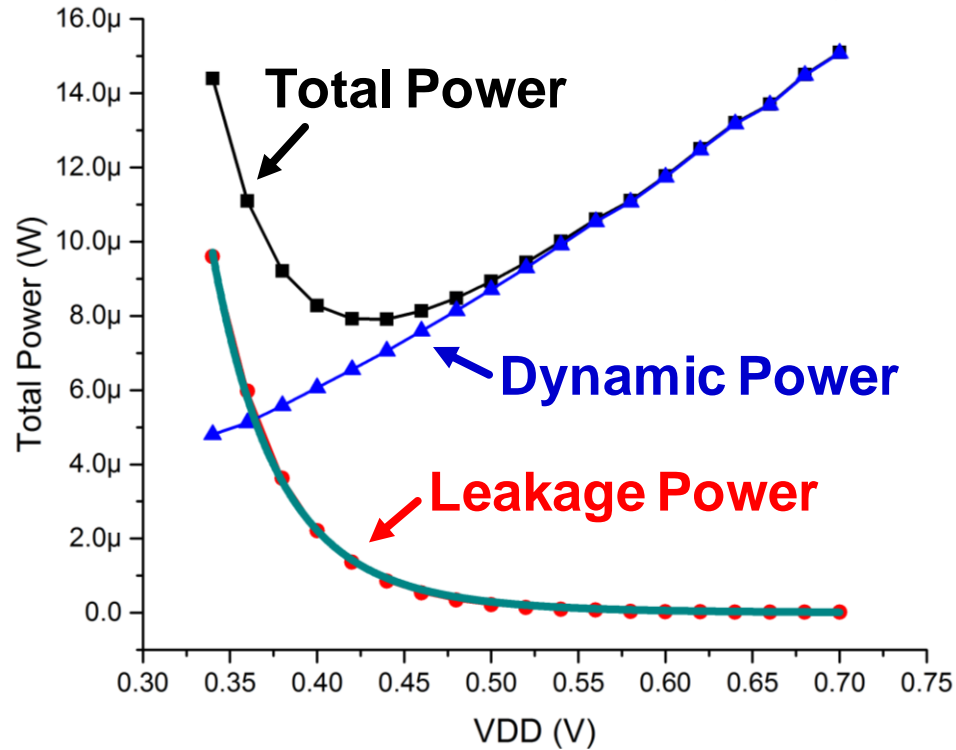


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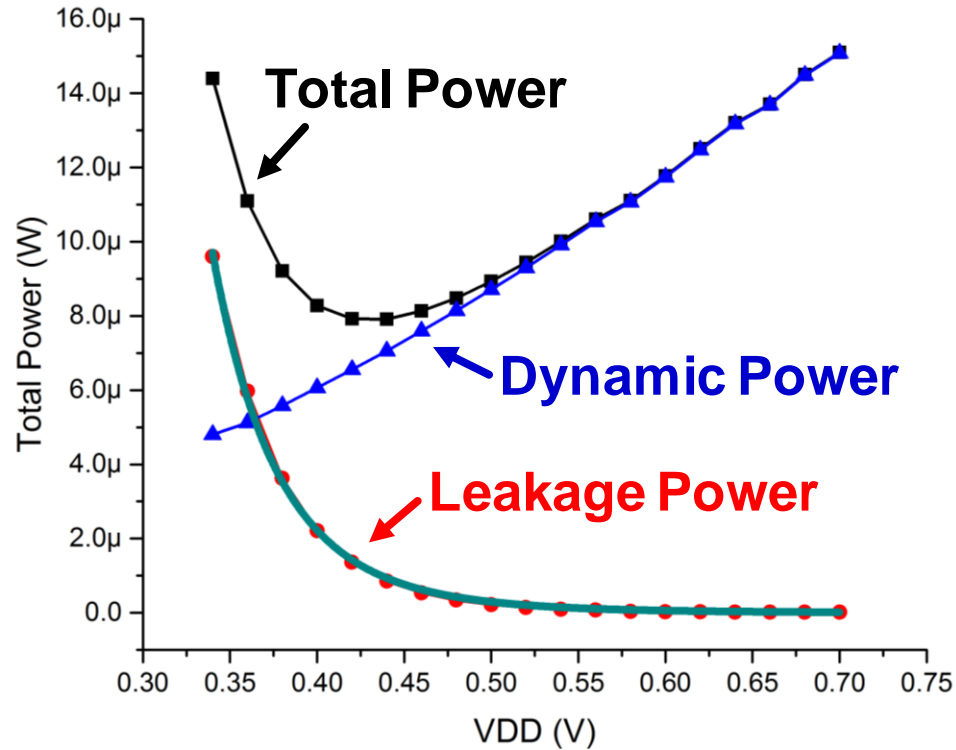


According to line fitting, $b \approx 9$

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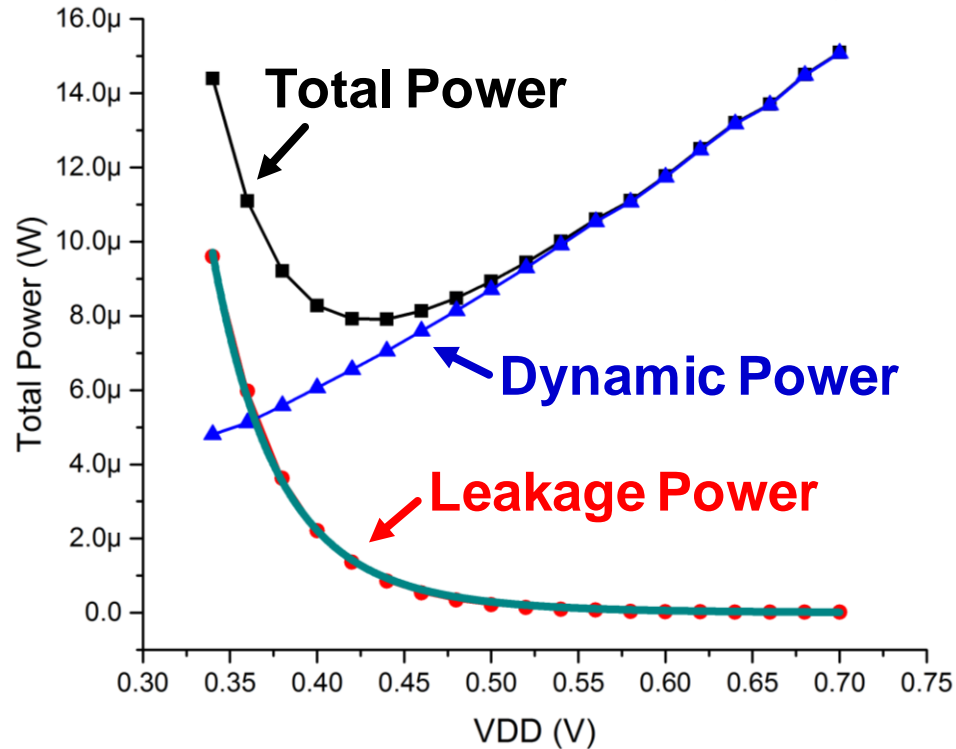
Since $P_{dyn} = cV_{DD}^2 f$ (c is *const.*)

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According to line fitting, $b \approx 9$

Assume $P_{leak} = aV_{DD}^{-b}$ (a, b is const.)

Since $P_{dyn} = cV_{DD}^2f$ (c is const.)

Then $P_{total} = aV_{DD}^{-b} + cV_{DD}^2f$

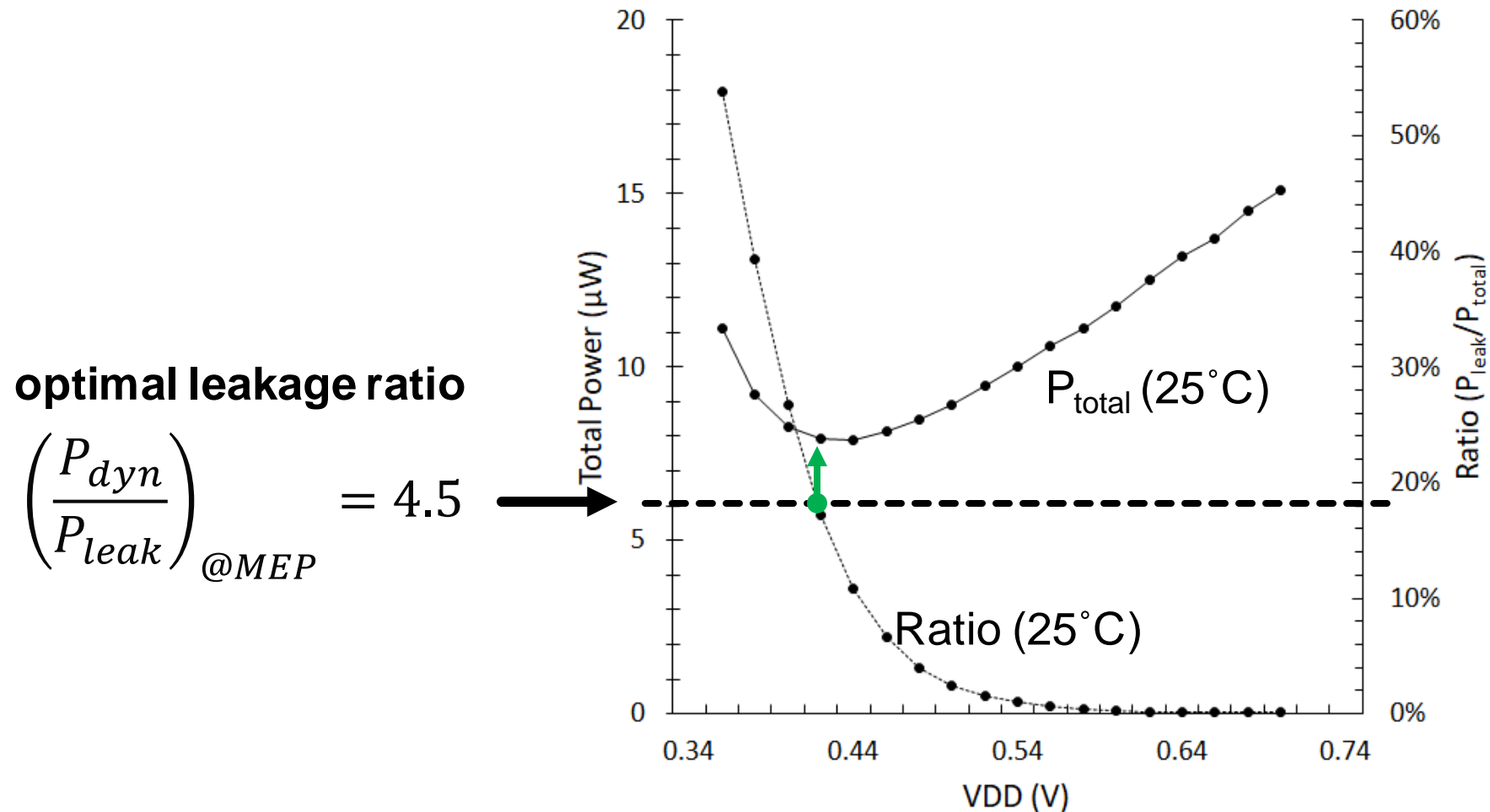
Minimize P_{total} : $\frac{dP_{total}}{dV_{DD}} = 0$

$$\Rightarrow -abV_{DD}^{-b-1} + 2cV_{DD}f = 0 \Rightarrow \frac{cV_{DD}^2f}{aV_{DD}^{-b}} = \frac{b}{2}$$

$$\left(\frac{P_{dyn}}{P_{leak}} \right)_{@MEP} = \left(\frac{cV_{DD}^2f}{aV_{DD}^{-b}} \right)_{@MEP} = \frac{b}{2} \approx 4.5$$

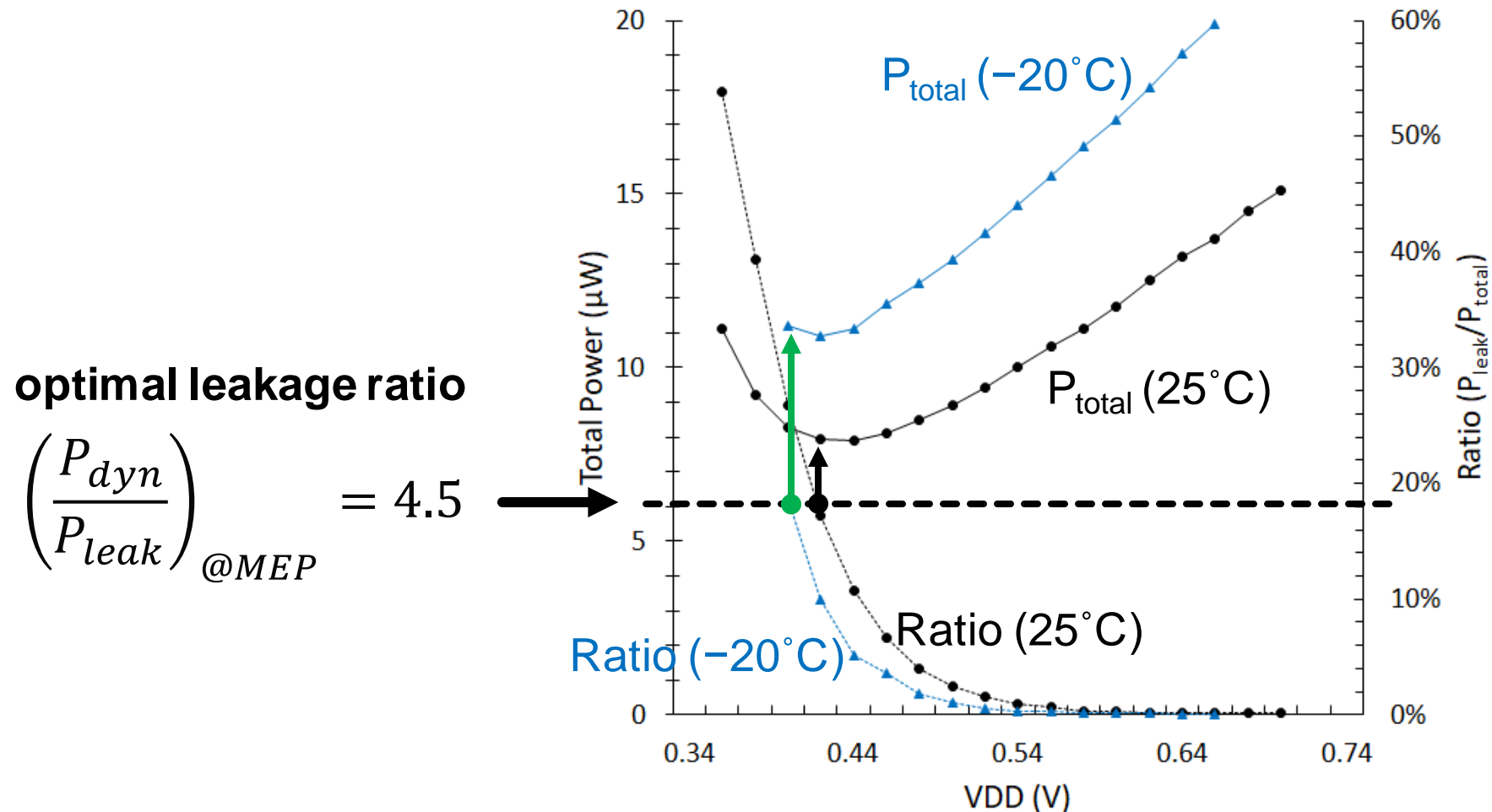
Key Observation: Optimal Leakage Ratio

- Verified optimal leakage ratio with simulation results



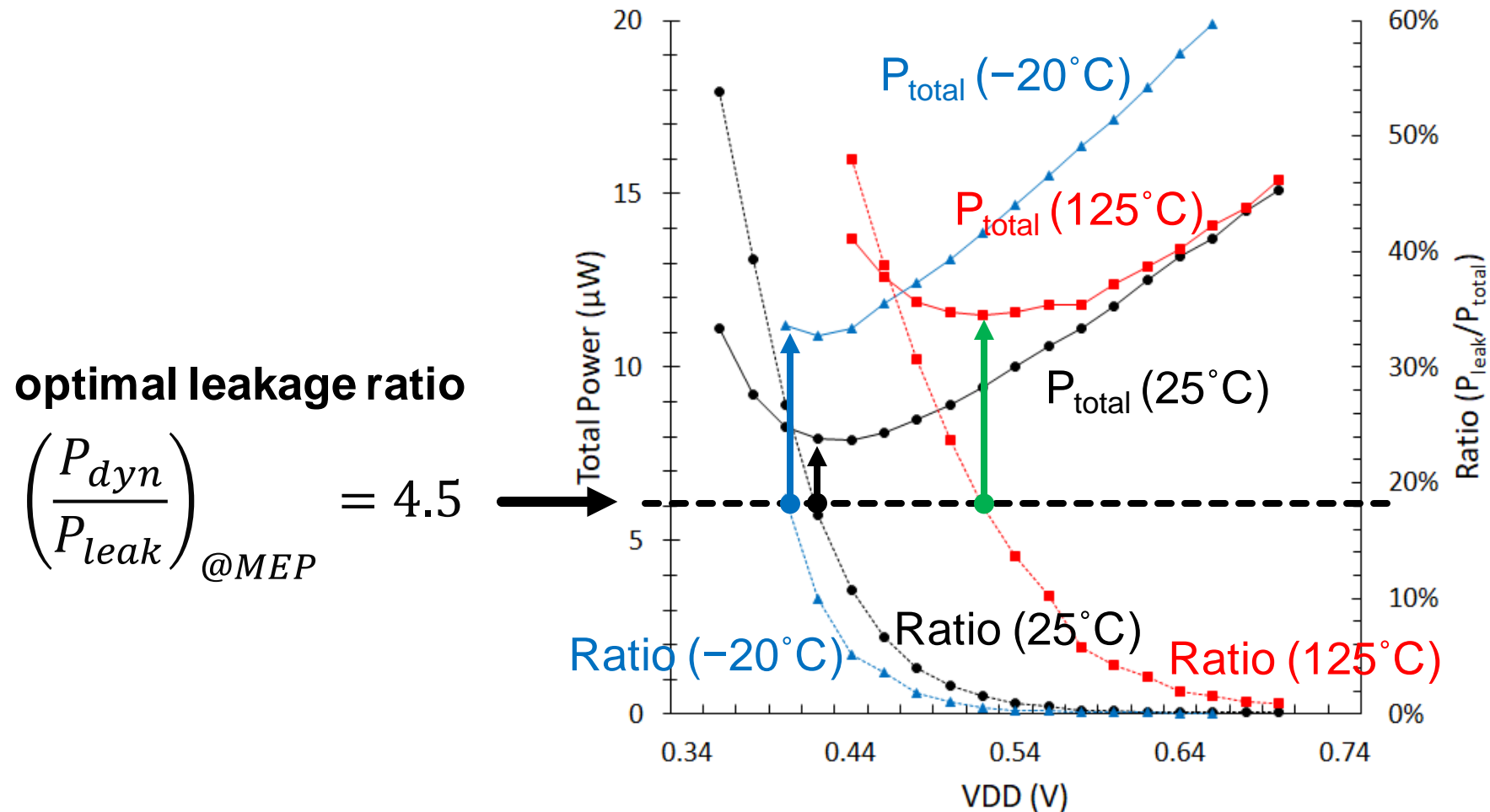
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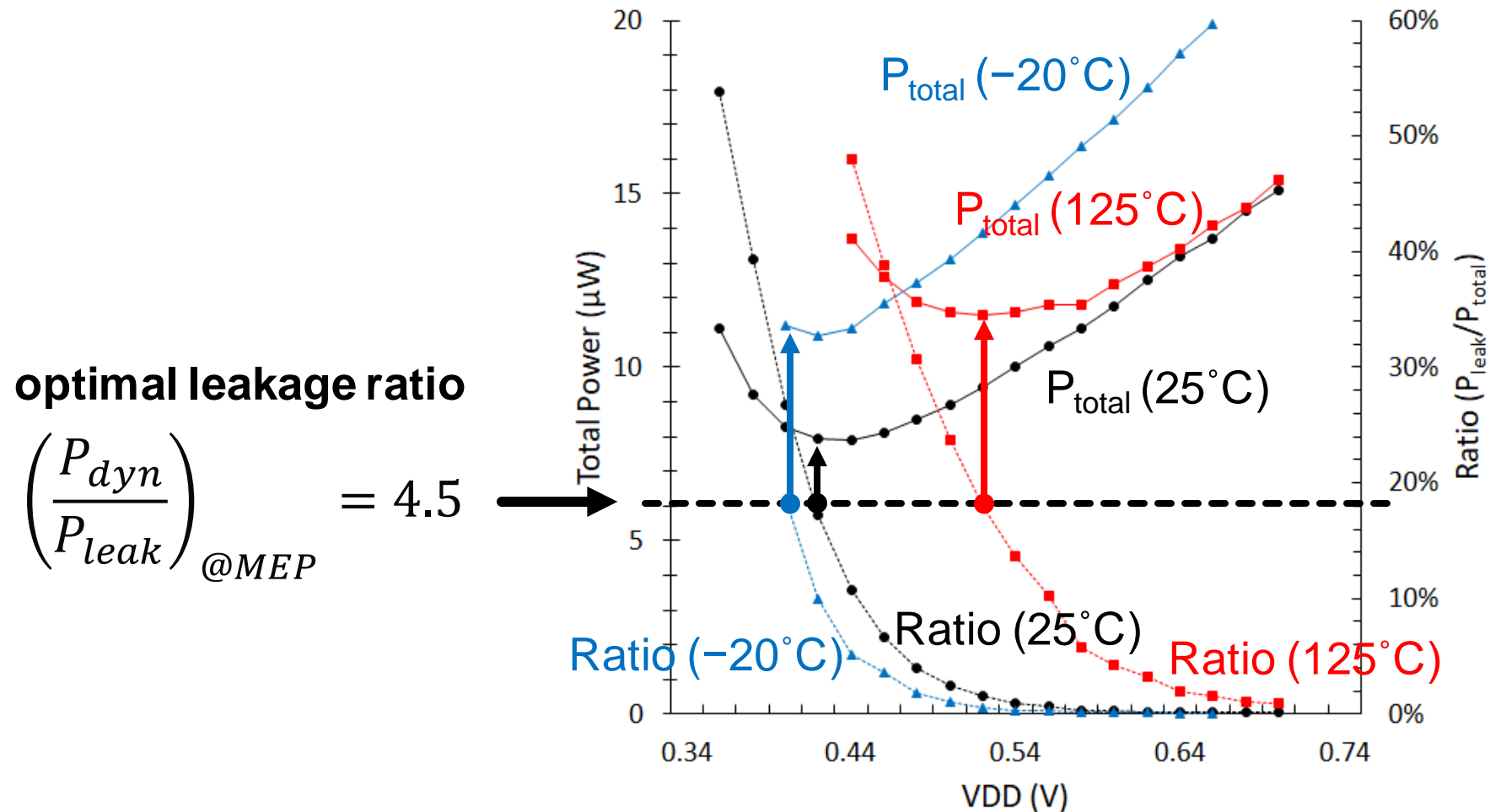
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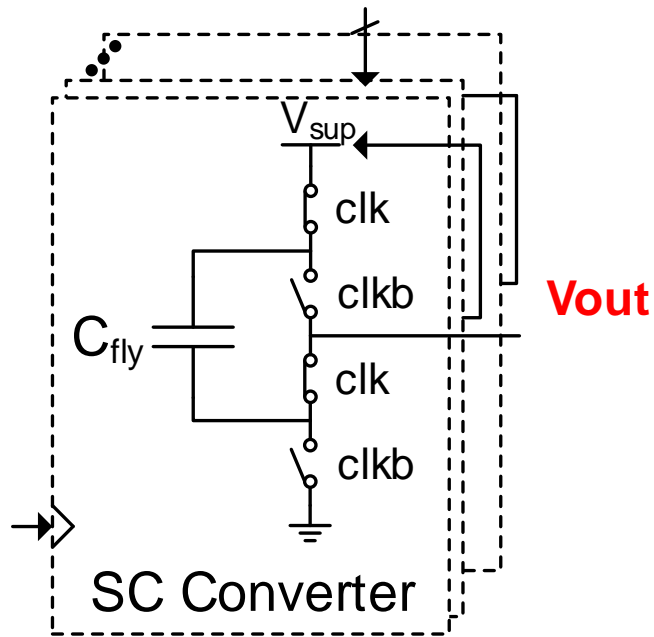
- 18% Ratio yields power within 2% from the minimum



How we measure leakage ratio

How to Measure $P_{\text{dyn}}/P_{\text{leak}}$

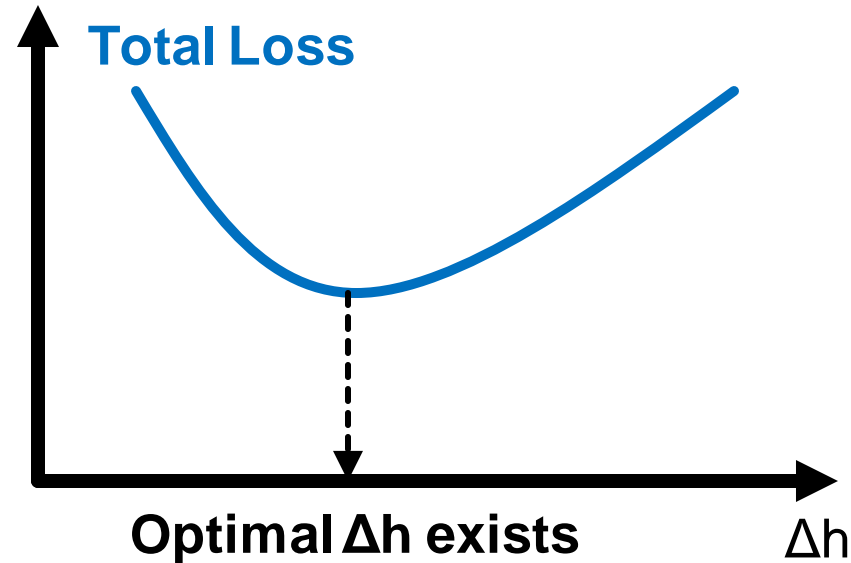
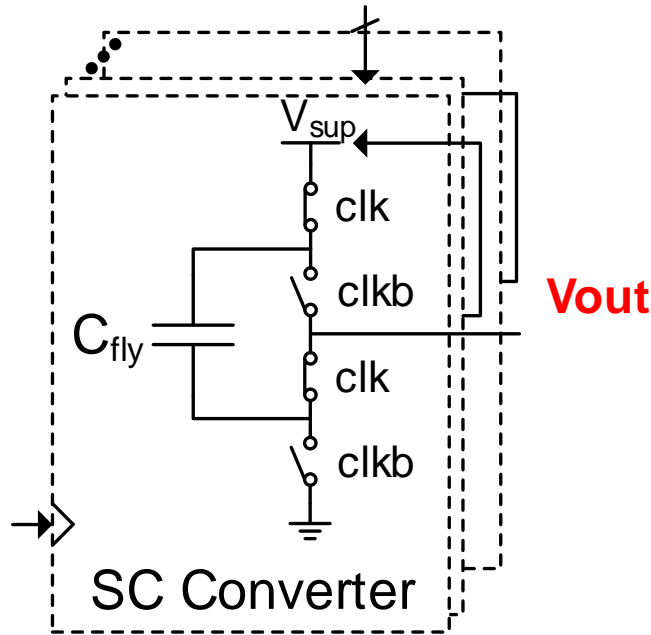
- ❑ Switched-cap DC-DC converter is commonly used



How to Measure $P_{\text{dyn}}/P_{\text{leak}}$

❑ Switched-cap DC-DC converter is commonly used

➤ Δh : **Output voltage without load** – **V_{out}**

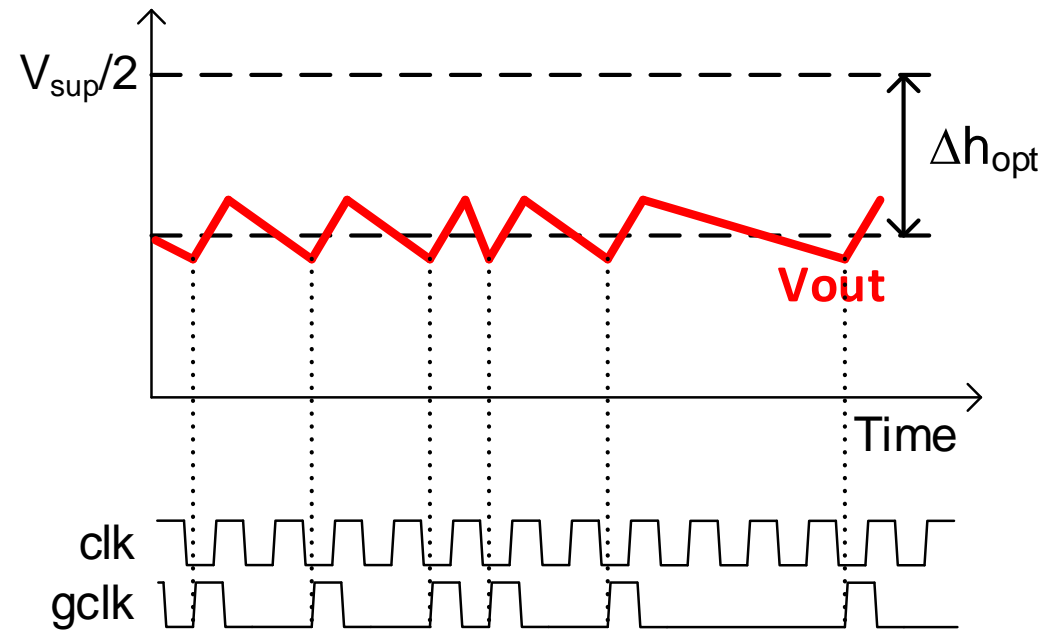
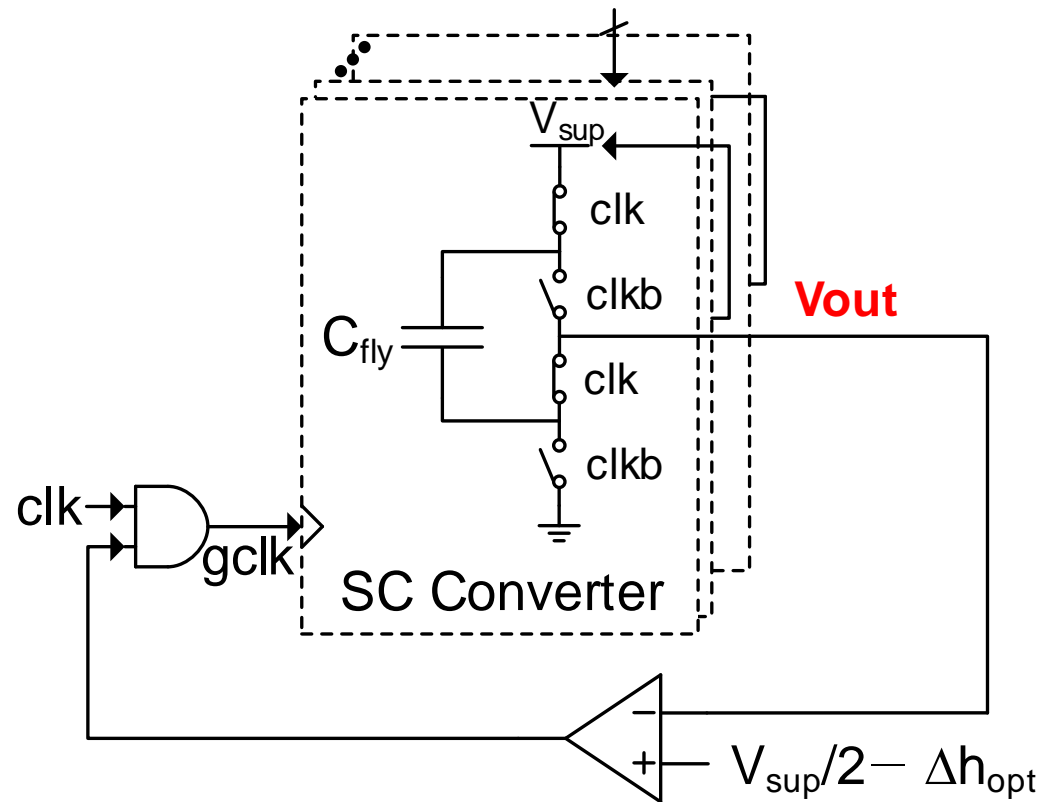


(which is constant and determined by C_{fly} and C_{para} [Ref])

[Ref] “An Ultra-Low Power Fully Integrated Energy Harvester Based on Self-Oscillating Switched-Capacitor Voltage Doubler”, Wanyeong Jung et al., JSSC2014

How to Measure $P_{\text{dyn}}/P_{\text{leak}}$

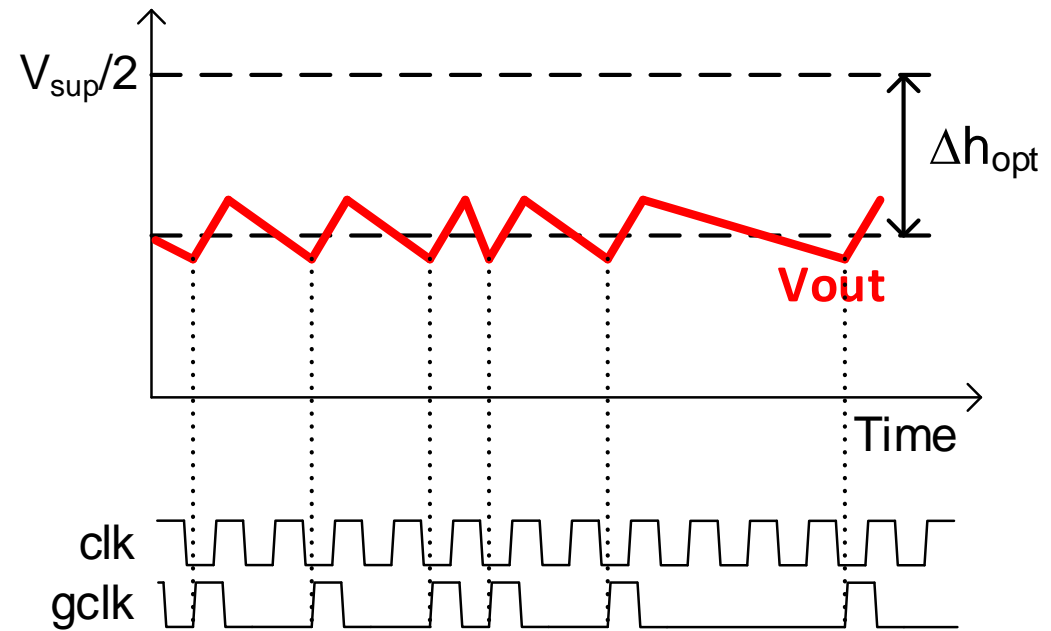
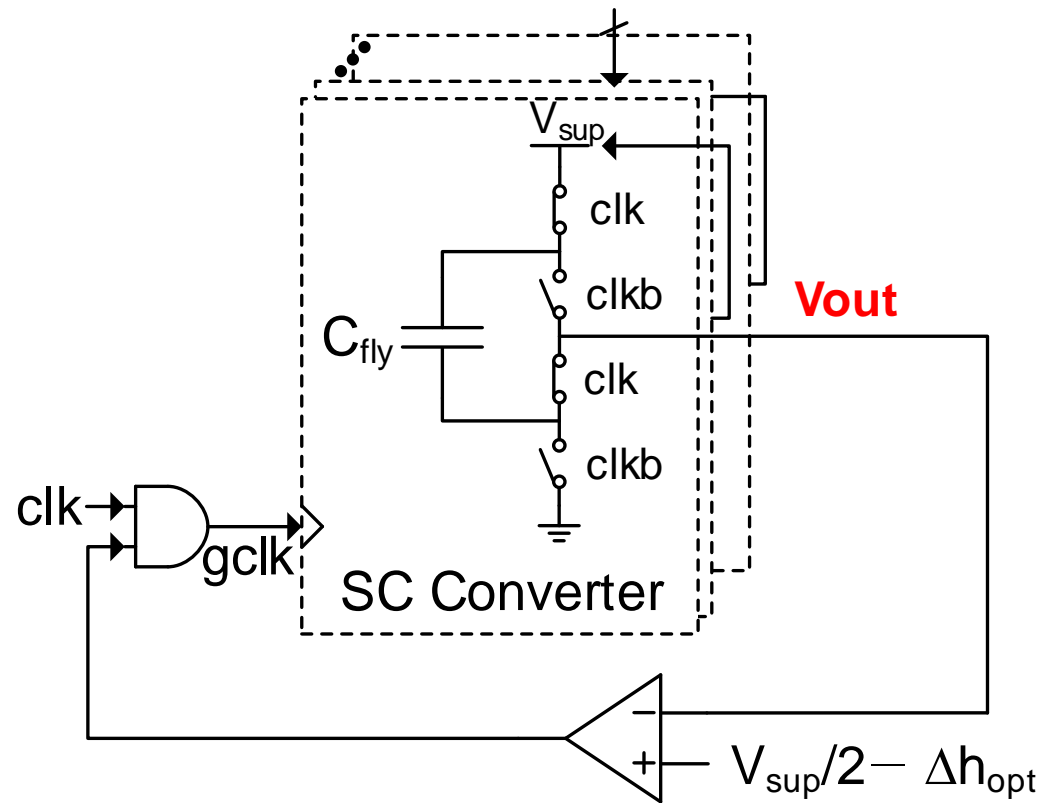
- ❑ Regulate Δh to be optimal Δh_{opt} by clock skipping
 - **Charge transfer per clock cycle** is constant: $\Delta Q = 4 \cdot \Delta h_{\text{opt}} \cdot C_{\text{fly}}$



How to Measure $P_{\text{dyn}}/P_{\text{leak}}$

□ Regulate Δh to be optimal Δh_{opt} by clock skipping

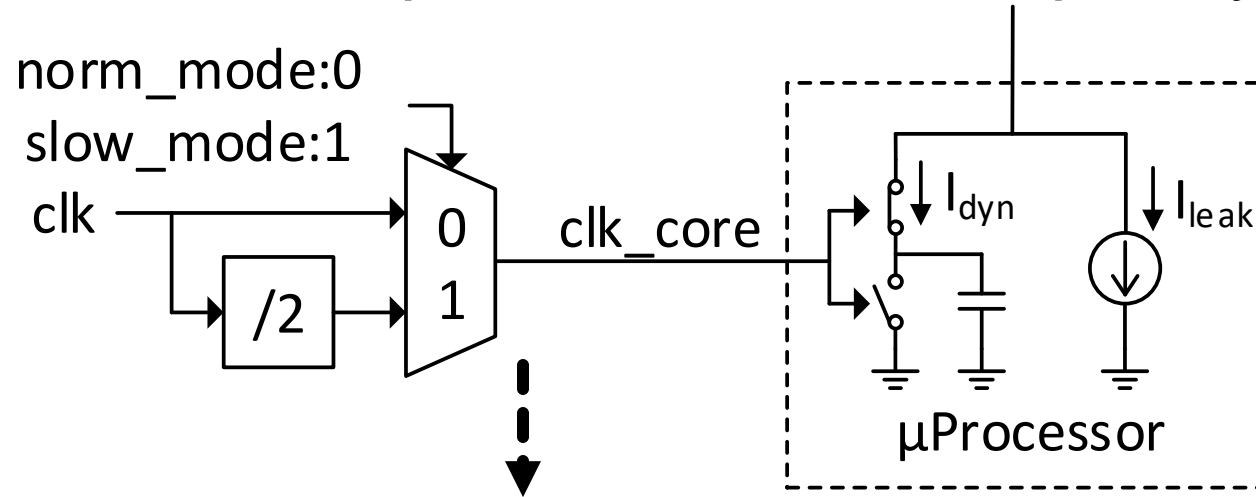
➤ **Charge transfer per clock cycle** is constant: $\Delta Q = 4 \cdot \Delta h_{\text{opt}} \cdot C_{\text{fly}}$



Count gclk to get $f_{\text{gclk}} \rightarrow I_{\text{load}} \propto f_{\text{gclk}}$

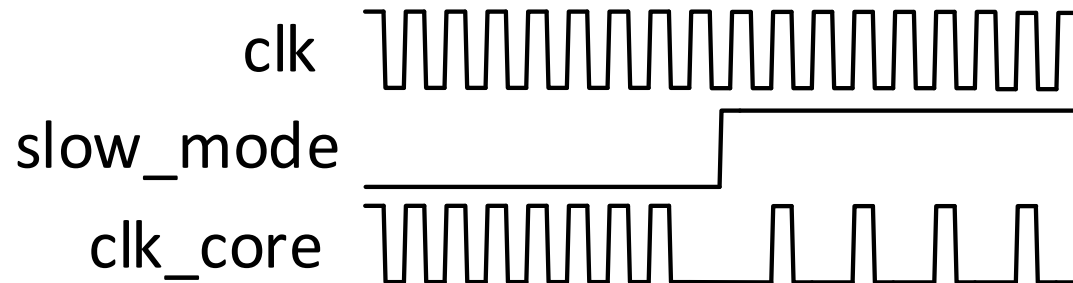
How to Measure P_{dyn}/P_{leak}

- ❑ Modulate processor clock frequency: **Normal & Slow mode**



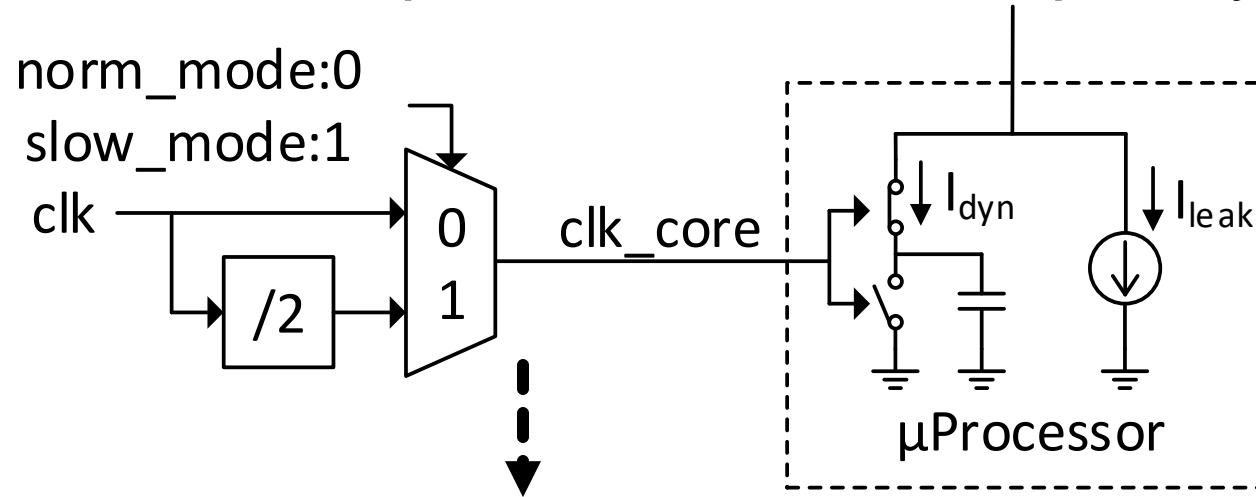
$$I_{load_norm} = I_{dyn} + I_{leak}$$

$$I_{load_slow} = \frac{I_{dyn}}{2} + I_{leak}$$



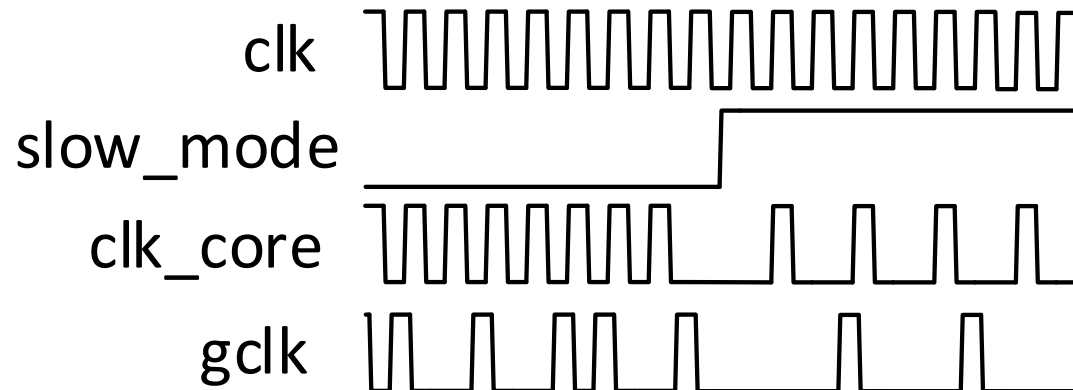
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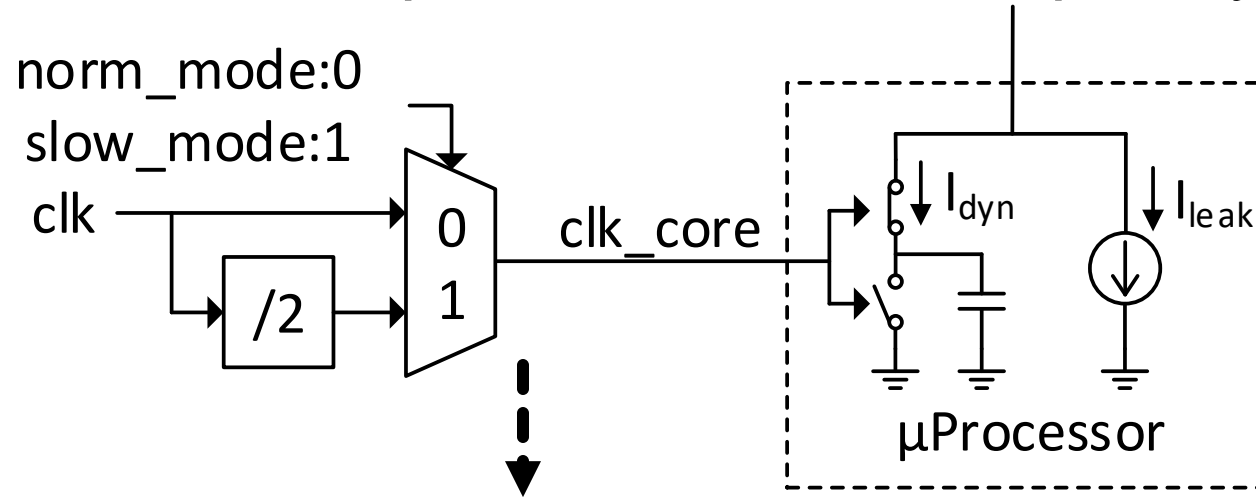
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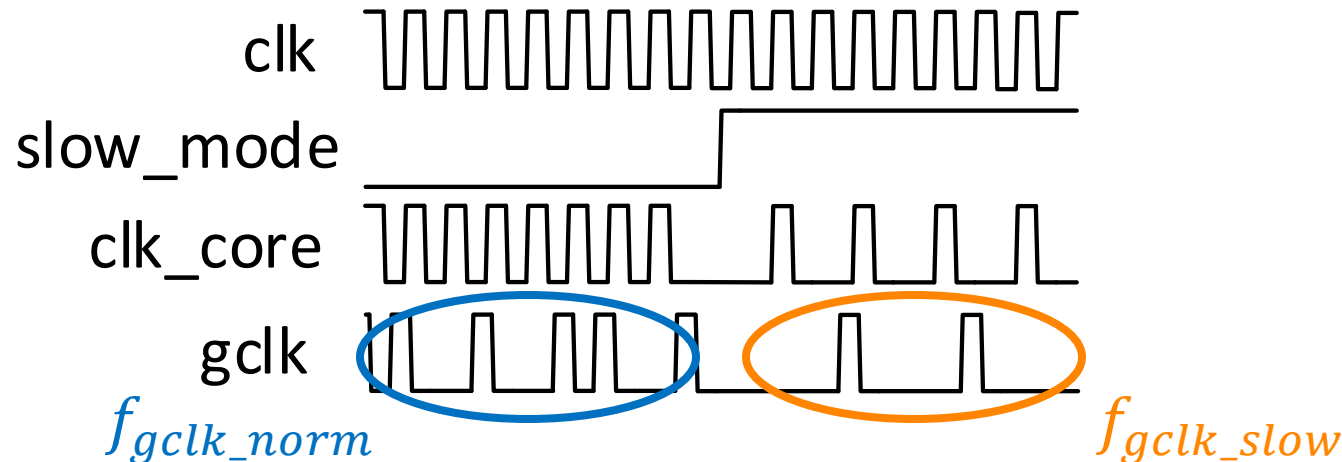
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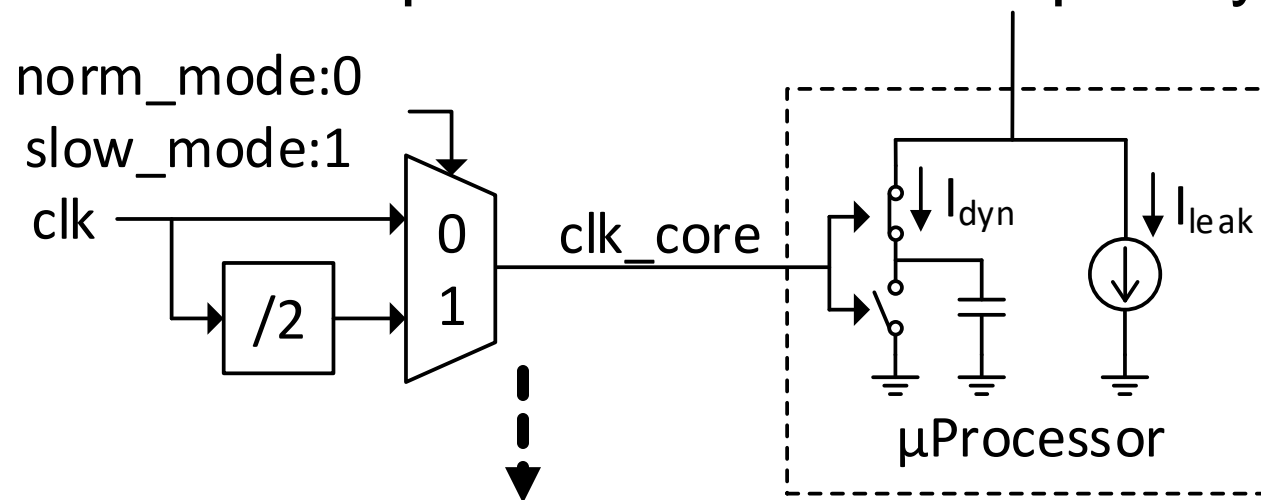
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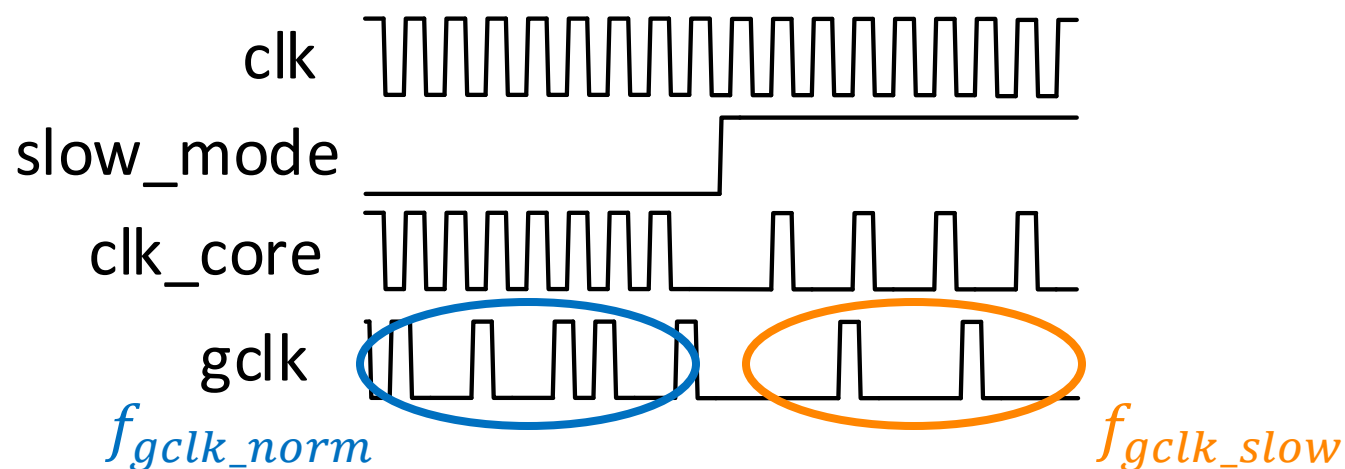
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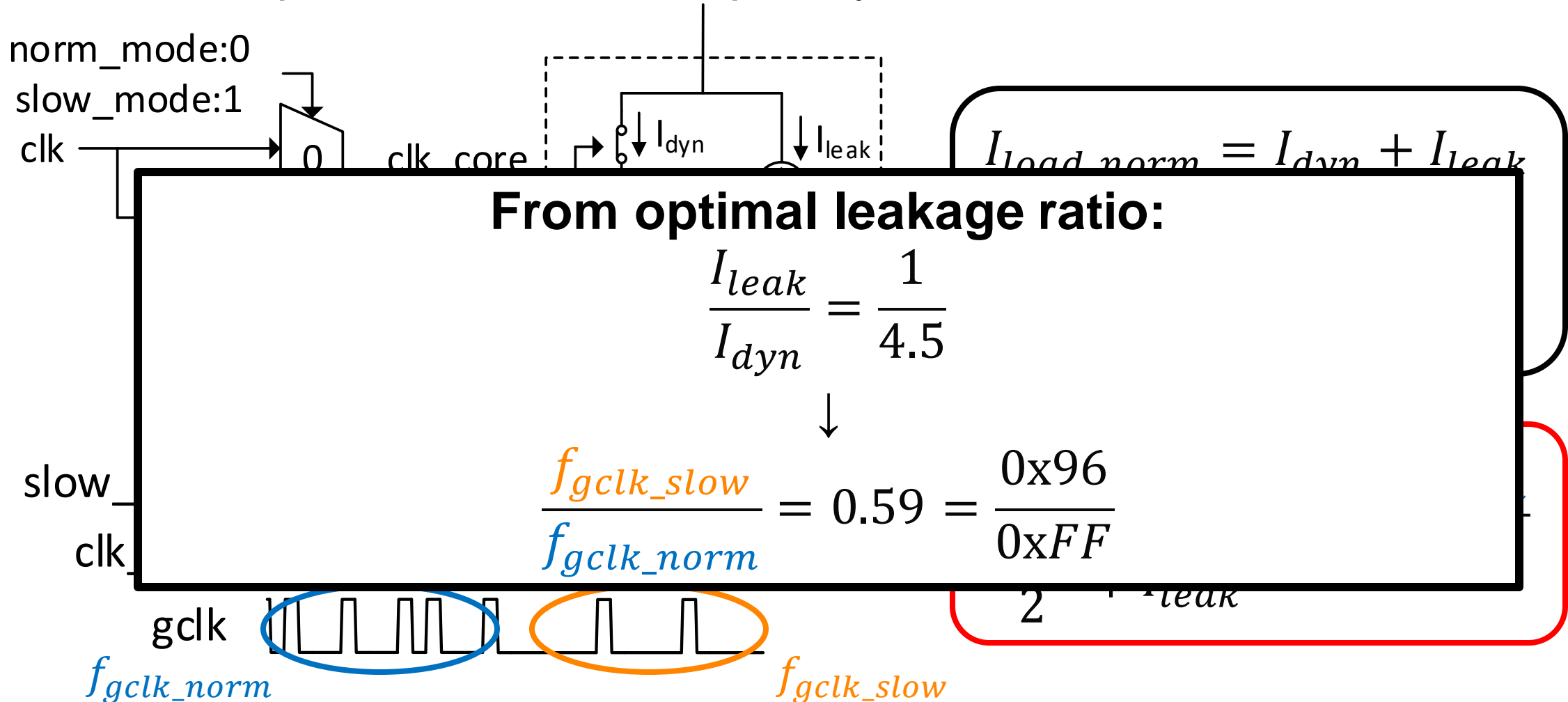
$$I_{load_slow} = \frac{I_{dyn}}{2} + I_{leak}$$



$$\frac{I_{dyn} + I_{leak}}{\frac{I_{dyn}}{2} + I_{leak}} = \frac{f_{gclk_norm}}{f_{gclk_slow}}$$

How to Measure $P_{\text{dyn}}/P_{\text{leak}}$

- ❑ Modulate processor clock frequency: **Normal & Slow mode**



Circuit Implementation & Measurements

Overall Block Diagram

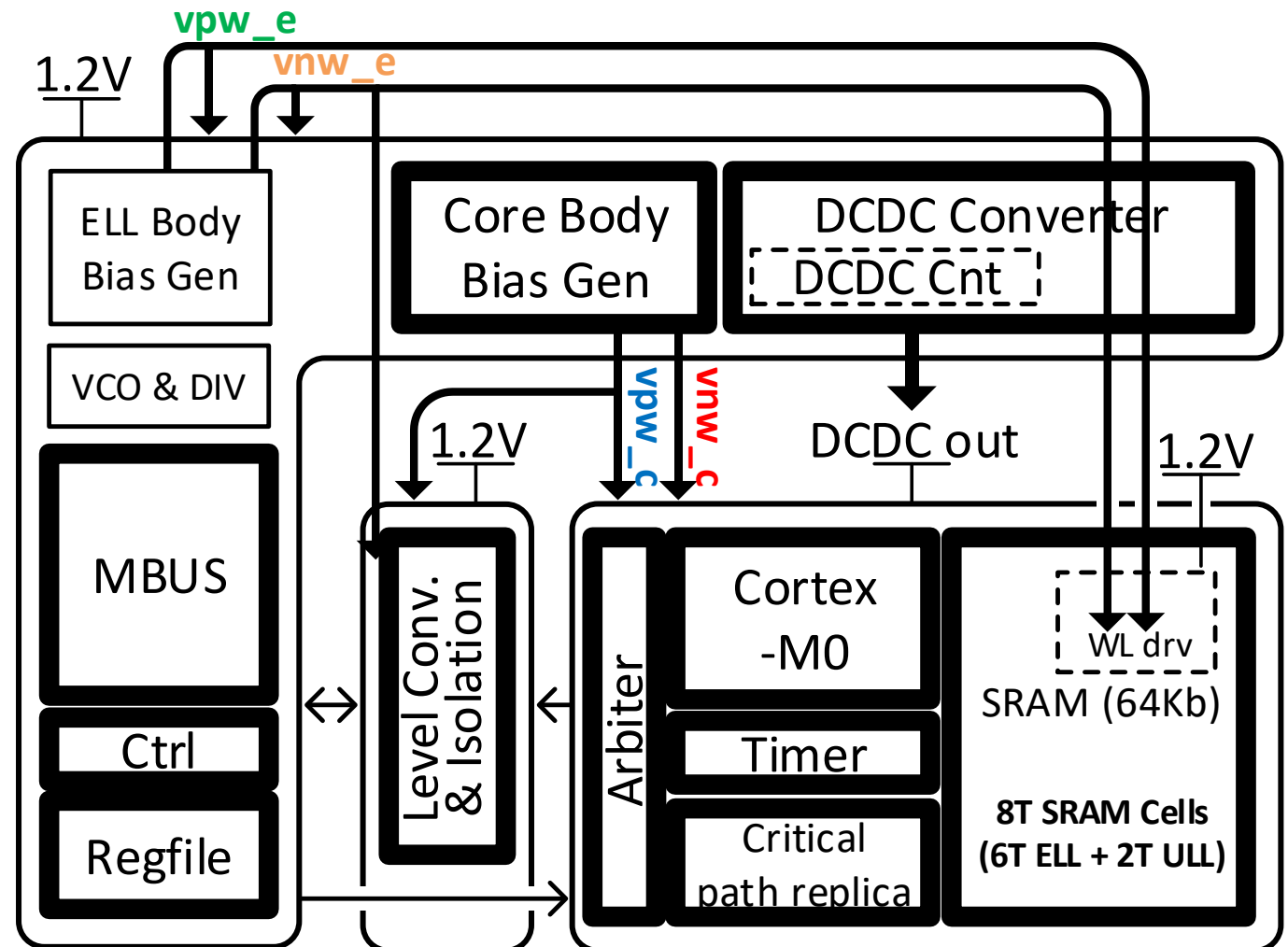
❑ Power domains

➤ 1.2V

- ✓ DC-DC converter
- ✓ Charge pumps
- ✓ Clock generator
- ✓ Controller

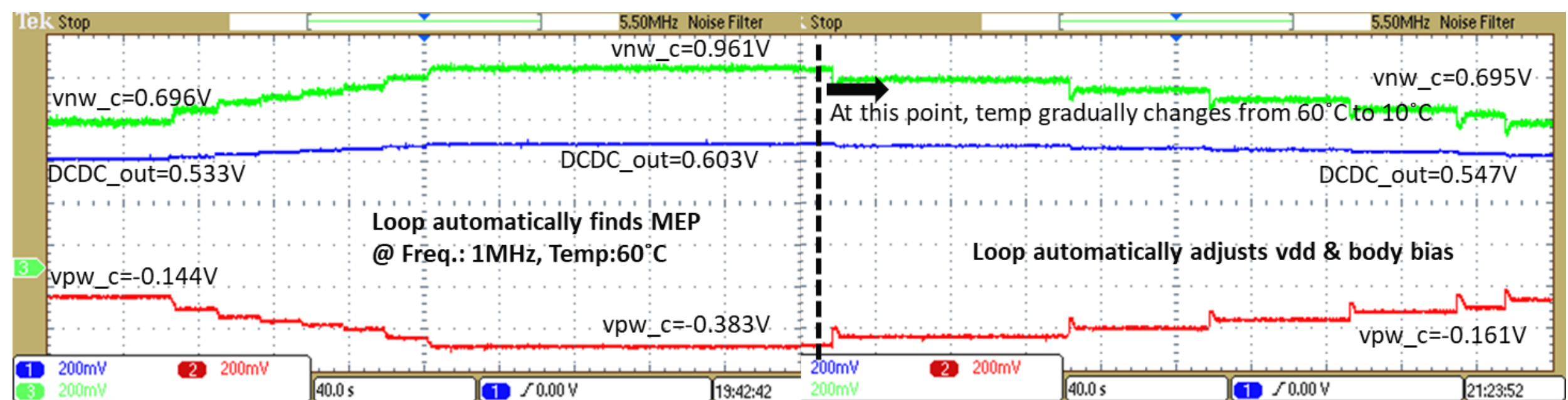
➤ DC-DC output

- ✓ Cortex-M0 processor
- ✓ 8KB SRAM



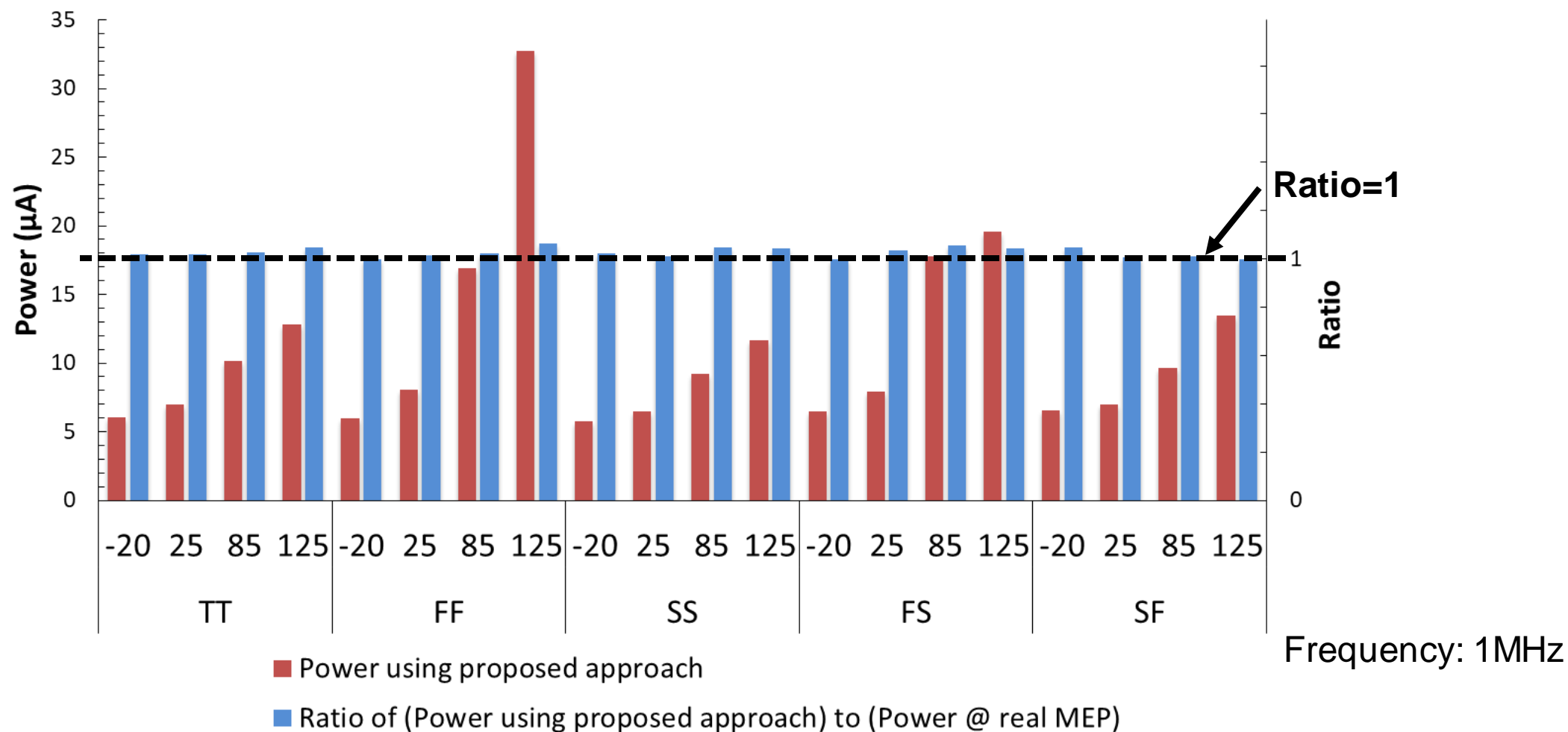
Measurement: Example Search Scenario

1. Start with the default setting
2. Find MEP @ Freq: 1MHz, Temp:60°C
3. Adjust MEP as Temp changes from 60°C to 10°C



Measurement: Power across P&T

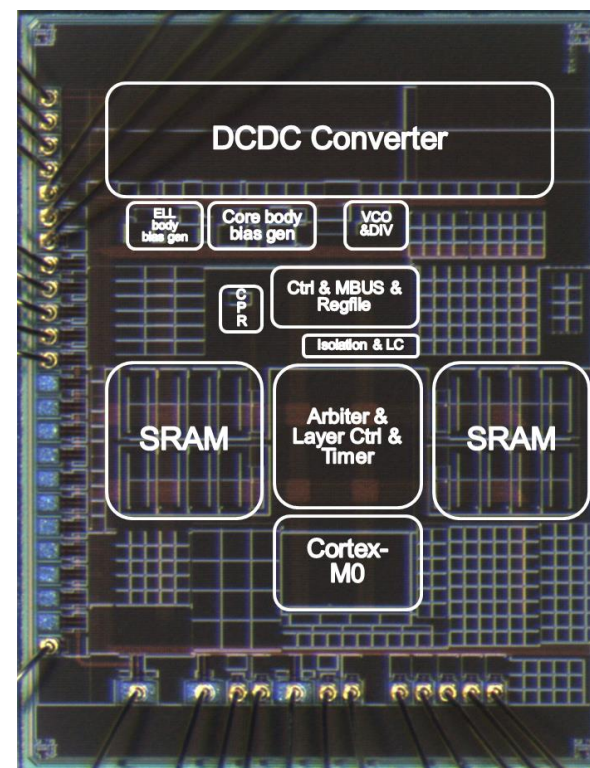
- Achieves power consumption within 4.6% of optimal



Chip Summary & Conclusion

- ❑ Introduce Optimal Leakage Ratio
- ❑ Implement runtime MEP tracking by measuring $P_{\text{dyn}}/P_{\text{leak}}$
 - Leverage frequency modulation in the embedded DC-DC

Technology	55nm DDC process
Die Size	1500μm x 1970μm
CPU	ARM Cortex M0
On-chip Memory	8KB SRAM
Supply Voltage	1.2V
Power Management Scheme	On-chip Closed-loop MEP-tracking
CPU & Memory Operating Voltage	0.48V ~ 0.75V
Clock Frequency	100kHz ~ 6MHz
Power	7.95μW @ TT, 25°C ,1MHz
Minimum Energy Per Operation	6.4pJ/cycle @ 0.55V, 500kHz



Thank you