AUTOSAR Safety Features and the ARMv8-R

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Outline

- Introduction
- Implementing AUTOSAR Safety Features
  - Memory Protection
  - Timing Protection
  - Core Error Detection
  - Memory Error Detection

- Conclusions

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Introduction

- ARM is developing a new processor architecture that is aimed to carry out features which will help in the task of providing solutions to the automotive market demands

- This presentation focuses on the implementation of AUTOSAR Safety Features using the ARM Cortex-R52

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ETAS

Implementing AUTOSAR Safety Features

- When implementing AUTOSAR safety features, following categories should be considered:

  - Isolation
  - Detection
  - Recovery

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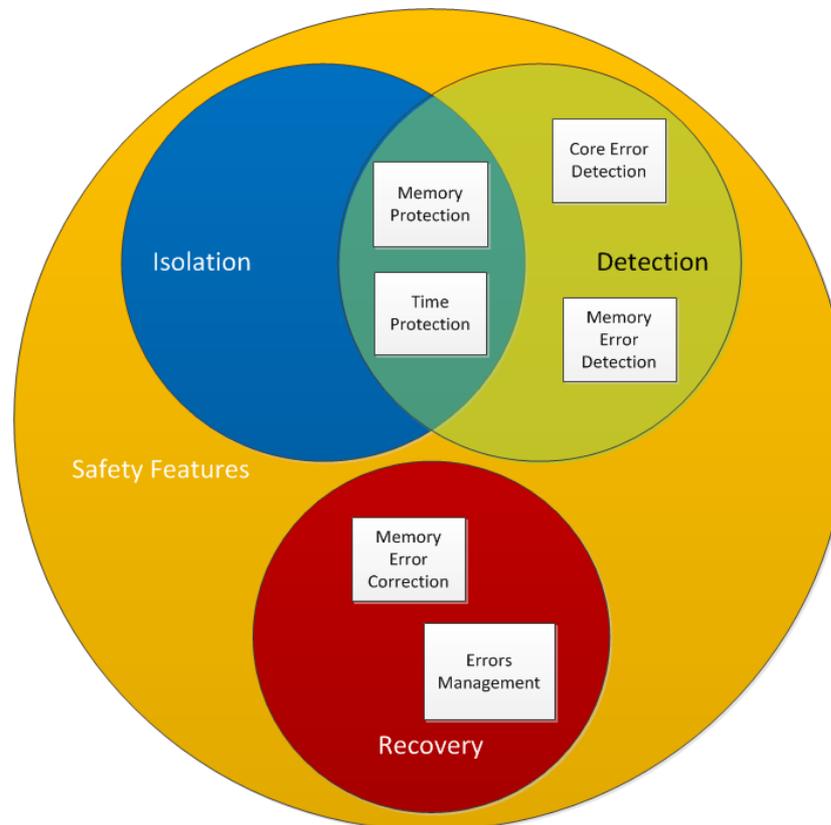
Memory Protection

- The AUTOSAR OS (SC4) must support memory protection

- In the Cortex-R52, there is a 2 stage MPU
- The OS can configure the stage-1 MPU to setup regions according to AUTOSAR partitions (OS-Applications)

- The OS can either select active regions at each context switch or reconfigure the MPU completely

- The MPU can be also used to setup attributes such as read, write, cacheable

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Time Protection

– The AUTOSAR OS (SC4) must support time protection

– In the Cortex-R52, there is a virtual timer concept
– The virtual timer configuration is left to the implementer

– All is needed to the AUTOSAR OS are some comparators which can trigger time events (i.e. used to issue hard time deadlines)

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Core Error Detection

- AUTOSAR Specifications include a CoreTest driver
- This is typically used where hardware support for core functionality test is not available

- In the Cortex-R52, the Dual-Core Lock-Step feature is supported
- Therefore no further software support is required

Cortex-R52 DCLS

Core

Checker Core

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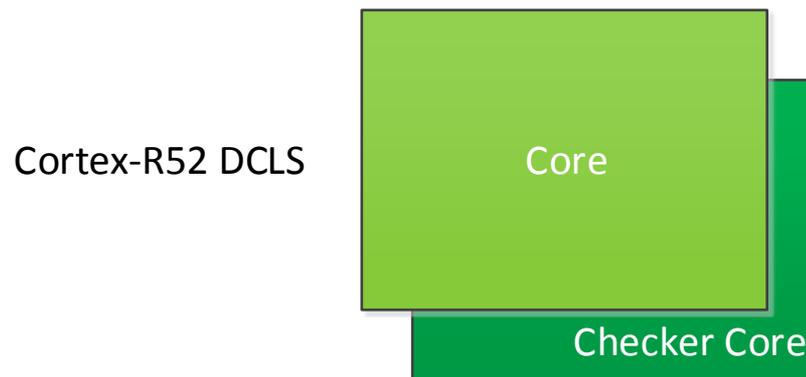
Memory Error Detection

– AUTOSAR Specifications include a RAMTest and FlashTest driver
– This is typically used where hardware support for memory test is not available

– In the Cortex-R52, the ECC feature is supported for RAM, ROM and buses (data/address)
– Therefore no further software support is required

– However, if some advanced functionalities are required, a complex driver could be implemented to support features such as error memory maps, warning events, etc.

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Conclusions

– The Cortex-R52 provides a full comprehensive solution for supporting AUTOSAR safety features

– Cortex-R52's key features
    – Two stages MPU
    – Virtual Timer
    – Core and memory diagnostic

Also, as part of the safety feature set, a BIST bus port is included in the Cortex-R52 for supporting off-line as well as on-line hardware testing (i.e. memory on-line testing)

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Thank you

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